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TERNARY LOGIC CIRCUITS USING CNTFET: A BRIEF REVIEW

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Abstract—A brief review about carbon nanotube is presented at first, followed by a brief review of ternary logic and then finally some of the ternary logic circuit built with carbon nanotube field effect transistor (CNTFET) are discussed. Recent progress in ternary logic circuit proposed by using CNTFET as basic building block is discussed in this paper. Complementary CNTFET designs are used to build ternary logic circuits just like Complementary CMOS designs. MVL has gained its popularity as binary logic circuits are reaching its limitations. Different CNTFET Ternary logic circuits like half adder (HA), full adder (FA) and multiplier circuits are studied and a brief review is presented in this paper about how different designs and different methodologies are proposed to achieve high performance, low power consuming and also with less delay.

Keywords—Binary Multiplexer; CMOS; CNTFET, MOSFET; MVL; Ternary logic; Ternary Decoder; Ternary Multiplexer.

I. INTRODUCTION

Binary logic has two logic values (logic 0 and logic 1) whereas MVL has more than two logic values i.e. Ternary logic has three logic values (logic 0, logic 1 and logic 2) while Quaternary logic has four logic values. Major problems with usage of two level logic are interconnection problem that arises inside the chip and also among the chips (Vudatha et al., 2013). As number of logic elements in the chip are increasing every year, positioning and interconnection of those logic elements are creating problems for the designers; chip area required for interconnecting logic elements are more than the area required for placing of all the logic elements (Hurst et al., 1984). Also, taking the increasing number of interconnection out of the chip for packaging is creating new challenges for industries (Hurst et al., 1984). Due to this binary logic has reached its limitations therefore it is required to have a logic level of radix greater than 2.

MVL raises data content per interconnection therefore, interconnection and insulation required can be reduced. As each pin are carrying more data, therefore number of pins required can be reduced, hence the complexity of the chips are reduced. Pin-out issue and number of associations inside the circuit could be considerably reduced if signals in the circuit

are permitted to expect more logic levels instead of two logic levels. (Dubrova et al., 1999).

As the number of transistors per unit area of the chip is doubling in every twelve months, various endeavours have been made to shrink the size of the MOSFET devices [Kim et al., 2010]. MOSFET device performance are hampered as the supply voltage (V_{DD}) approached to 1V; therefore, further lowering of threshold voltage (V_{th}) is difficult (Kim et al., 2010). Lowering of threshold voltage leads to subthreshold leakage current increase exponentially as V_{th} decreases. Therefore, it become necessary to determine lowest possible value of V_{th} for ideal working of MOSFET devices (Kim et al., 2010).

Threshold voltage brings new challenges therefore; a new technology is required to acknowledge these challenges. CMOS technology enabled scaling of MOSFET transistors from micrometre to sub-100nm regime. As silicon device scaling reaches sub-100nm regime device performance are hampered by short-channel effect (Kim et al., 2010). As CMOS devices are reaching its limitation many researchers had made efforts to find a way to take benefits of ballistic transport characteristics and quantum mechanical phenomena for these nano devices under low power consumption. Lots of new nano-electronic devices are introduced such as Nanowire (NW) transistors, Carbon Nanotube Field Effect Transistor (CNTFET), Graphene Nanoribbon (GNR) Transistors, Single Electron Transistor, Quantum Dot Cellular Automata (Kim et al., 2010). Carbon nanotube was introduced in 1991 (Iijima et al., 1991). CNTFET are most popular among the nano-electronic device because of its operating principle similar to that of CMOS transistors. CNTFET with different threshold voltages (V_{th}) (Multi-threshold CNTFET) can be attained by varying CNT's diameter. Properties like high thermal conductivity, exceptional mechanical stability, thermal stability and large current carrying ability makes CNTFET's more popular (Kim et al., 2010).

II. CARBON NANOTUBE FIELD EFFECT TRANSISTOR

Carbon Nanotube (CNT) is a long hollow tube that is done by wrapping a graphene sheet. Graphene is honey comb sheet of carbon atom which is one atom thick. Chemical bonding of nanotube is composed of sp^2 bonds (Iijima et al., 1991).

Single Walled CNT (SWCNT) and Multi Walled CNT (MWCNT) are the types of CNT's. Single Walled CNT (SWCNT) comprise of single graphene sheet wrapped in the form of a tube, whereas Multi Walled CNT (MWCNT) comprise of several sheets of graphene wrapped in a tube form (Iijima et al. and Iijima et al., 1991,1993). Diameter of MWCNT can be in tens of nanometre, while diameter of SWCNT can be one or five nanometres. The direction of wrapping of graphene sheet to form CNT decides whether the nanotubes are of metallic nature or semiconducting nature. The chirality indexes (n, m) of nanotube describes the direction of wrapping, where m and n are integers. Metallic or semiconducting behaviour of nanotube can be resolved by its index (n, m). Nanotube is metallic in nature if n is equal to m i.e. (n = m) or difference of n and m is equal to 3i i.e. (n - m = 3i), where 'i' is an integer; otherwise CNT is of semiconducting nature (Stanford University CNFET Model et al.).

Depending upon the chirality CNT is classified as chiral, zig-zag or armchair nanotube which has metallic or semiconducting characteristics (Collins et al., 2001). CNTFET's are of three types: - SB (Schottky barrier) CNTFET, BTBT (Band to band tunnelling) CNTFET, Metal Oxide Semiconductor Field Effect Transistor (MOSFET) like Carbon Nanotube Field Effect Transistor (CNTFET). MOSFET's like CNTFET's have similar characteristics to that of MOSFET's (Das et al., 2018). Therefore, MOSFET like CNTFET are most popular among all other types of CNTFET's. Diameters of CNT can be calculated by (Stanford University CNFET Model et al.), (Deng et al. and Deng et al., 2007,2007): -

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi} \sqrt{m^2 + n^2 + mn} \quad (1)$$

Where $a_0 = 0.142$ nm is interatomic distance among neighbouring carbon atoms.

CNTFET threshold voltage can be changed by varying the diameter of CNT's. Therefore, to accomplish multi-threshold CNTFET's with different diameters are used. The threshold voltage of the CNTFET can be changed by altering the chirality vector. If we assume chirality vector m to be zero, then threshold voltage ratio of two CNTFET's with unlike chirality vector is given by (Raychowdhury et al., 2005): -

$$\frac{V_{th1}}{V_{th2}} = \frac{D_{CNT2}}{D_{CNT1}} = \frac{n_2}{n_1} \quad (2)$$

From equation (4) it is clear that diameter (D_{CNT}) and chirality vector (n) both are in inverse proportion with V_{th} . Therefore, it is possible to vary the V_{th} of the CNTFET by varying chirality vector (n) or D_{CNT} (CNT diameter) (Raychowdhury et al., 2005).

III. REVIEW OF TERNARY LOGIC

Ternary logic is three level logic. These levels are logic 0, 1 and 2; where logic 0 is for 0 V (false), logic 1 is for $0.5 \times V_{DD}$

(intermediate) and logic 2 is for V_{DD} (true) (Vudadha et al., 2013). Ternary logic inverters are of three types depending upon the diameters of CNTFET's used as pull up or pull down devices (Das et al., 2018): -

- Standard ternary inverter
- Positive ternary inverter
- Negative ternary inverter

Ternary inverters output for input 'a' is given by (Das et al., 2018): -

$$STI = 2 - a \quad (3)$$

$$PTI = \begin{cases} 0, & \text{if } a = 2 \\ 2, & \text{if } a \neq 2 \end{cases} \quad (4)$$

$$NTI = \begin{cases} 2, & \text{if } a = 0 \\ 0, & \text{if } a \neq 0 \end{cases} \quad (5)$$

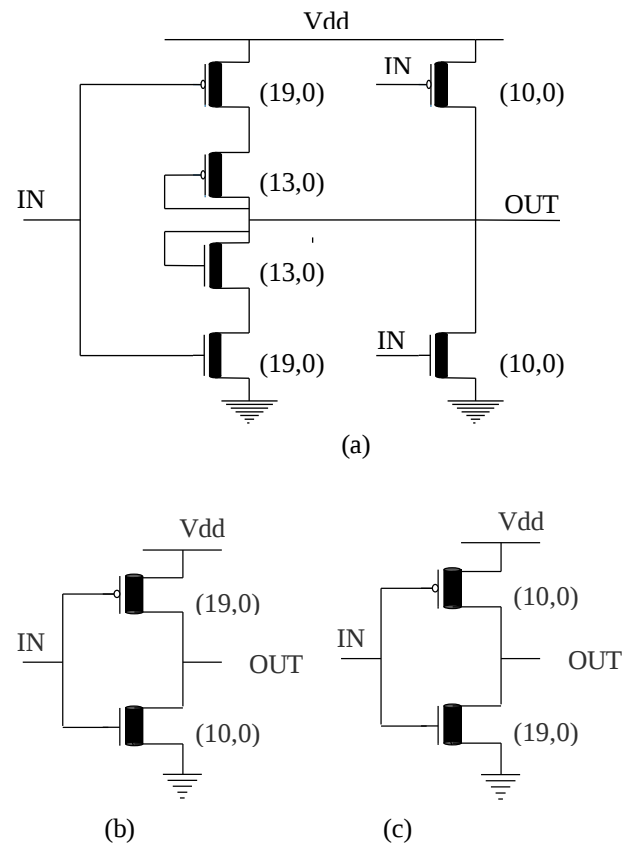


Fig. 1. (a) STI (b)PTI (c) NTI

Ternary inverters are presented in figure 1. Truth table showing the outputs of ternary inverters for ternary inputs are presented in table 1. Equations for ternary NAND and ternary NOR gates are (Heung et al., 1985): -

$$NAND = \overline{min\{x_1, x_2\}} \quad (6)$$

$$NOR = \overline{\max\{x_1, x_2\}} \quad (7)$$

Where x_1 and x_2 are two inputs. Therefore, ternary AND gate is known as Minimum gates and ternary OR gate is known as Maximum gates (Heung et al., 1985). Ternary AND and OR gates are defined as:

$$AND = \min\{x_1, x_2\} \quad (8)$$

$$OR = \max\{x_1, x_2\} \quad (9)$$

Table-1 Ternary inverters output for three level inputs

Input	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

Ternary decoder circuit takes one input and produces unary output for each input levels; therefore, for ternary logic three unary outputs are generated by this decoder. By using ternary decoder, use of binary gates are possible in ternary logic circuit design as this decoder converts ternary logic into binary (Lin et al., 2011). Ternary decoder circuit is shown in figure 2 (Lin et al., 2011).

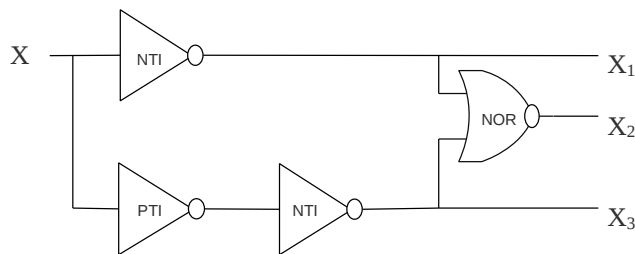


Fig. 2. Circuit diagram of Ternary Decoder

IV. CNTFET BASED TERNARY LOGIC CIRCUITS

In (Raychowdhury et al., 2005) ternary inverters are presented circuits with CNTFET's (Single Walled CNT) and resistive pull ups. Two resistors with value greater than 100 MΩ are used in this circuit design, which is too large to be used in nano devices. Also use of resistors consumes large area and power consumption is more. In (Lin et al., 2011) ternary inverter circuit is designed using complementary CNTFET's. Complementary CNTFET are similar to complementary MOS, CMOS are used to remove the use of large resistors. By using complementary CNTFET like CMOS power consumption can be reduced also performance of circuit can be improved. Ternary inverters with complementary CNTFET design style performance of inverters is higher, power consumption reduced and small area is required to built the circuit due to removal of large resistors. Therefore a complementary CNTFET design style just as CMOS design style can be used to design ternary logic to attain better performance, reduced

power and most importantly to eliminate the usage of resistors which increase the area required by the circuit.

In (Dande et al., 2005) ternary half adder circuit is presented which is built with ternary gates. In (Lin et al., 2011) ternary half adder circuit is presented which is built with both binary and ternary gates. Ternary logic decreases the total number of computation steps required, as ternary logic has three logic levels therefore, digits necessary in ternary logic is fewer than binary logic by $\log_3 2$. Binary logic is good for the units that needs fast computing; therefore designs built with both binary and ternary logic achieves better performance. Ternary half adder proposed in (Lin et al., 2011) is faster than proposed half adder in (Raychowdhury et al., 2005) with pull up resistors also with proposed half adder in (Dande et al., 2005) due to the use of binary gates number of transistors required is less that significantly reduces the power consumption and delay.

In (Vudadha et al., 2012) ternary half-adder circuit is built with ternary multiplexer. Ternary multiplexer consist of ternary decoder, three pass transistor and three inverters. In this circuit design four ternary multiplexers are used due to which large number of transistors are required which significantly increases the delay and power consumption. In (Vudadha et al., 2013) in this proposed design 2x1 mux with some additional circuitry are used to remove some of the 3x1 mux from the design proposed in (Vudadha et al., 2012), due to this number of transistors can be reduced. In (Vudadha et al., 2013) instead of four 3x1 mux, two 3x1 mux and two 2x1 mux with some additional circuitry are used to built ternary half adder circuit. This design consumes less power and delay is also reduced than design proposed in (Lin et al., 2011)(Vudadha et al., 2012).

Table-2 PDP of ARITHMETIC CIRCUITS (Lin et al., 2011)

Arithmetic Circuit	Ref (Lin et al., 2011)	Ref (Dande et al., 2005)	Ref (Raychowdhury et al., 2005)
Half Adder	0.411e-15	0.543e-15	6.17e-15
Multiplier	0.248e-15	0.261e-15	2.62e-15

Table-3 Simulation results of ternary half adder (Vudadha et al., 2013)

	Delay	Avg. power	Power Delay	Number of Transistors
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	(s)	consumption (W)	Product (PDP) (J)	required
Half adder (Lin et al., 2011)	35.49×10^{-12}	0.659×10^{-6}	2.338×10^{-17}	84
Half adder (Vudadha et al., 2012)	49.75×10^{-12}	0.929×10^{-6}	4.622×10^{-17}	77
Half adder (Vudadha et al., 2013)	42.82×10^{-12}	0.382×10^{-6}	1.636×10^{-17}	60
Half adder (Vudadha et al., 2013) with output STI gates	32.25×10^{-12}	0.678×10^{-6}	2.187×10^{-17}	66

In (Ebrahimi et al., 2012) ternary full adder is built with two half adder and a carry generator. In (Moaiyeri et al., 2011) two designs of ternary full adder is proposed. In first design five capacitors and 24 CNTFET transistor produce the inverse function of both sum and carry, therefore two inverters are used to produce the sum and carry from the inverse function. Distance among the input terminal and output terminal is large and also use of capacitor leads to more delay and leads to increase in power consumption. In second design 5 capacitors and 18 transistors are used. It reduces the distance among the input terminal and output terminal but still capacitors used leads to increase in delay and consumes more power. Power consumption of second design is more than the first because of the use of two buffers but delay is less than first design. In (Ebrahimi et al., 2012) ternary half adder circuit is proposed without capacitors due to which it consumes less power and also delay is less. Due to capacitors parasitic effect increases and noise margin decreases.

In (Keshavarzian et al., 2014) ternary full adder circuit is proposed with a sum generation circuit and a carry generation circuit. In this circuit input terminal and output terminal are close to each other i.e. distance among them are reduced and also capacitors are eliminated in this proposed circuit. This circuit consumes less power and delay is also less compared to the circuit proposed in (Ebrahimi et al., 2012)(Moaiyeri et al., 2011). In (Sahoo et al., 2017) carry generation unit is proposed

with reduced number of transistors than of (Keshavarzian et al., 2014), sum generation unit is same as it is proposed in (Keshavarzian et al., 2014). In carry generation unit some modifications are done so as to provide different path for different combination of inputs. Due to reduction in number of transistors, delay of the circuit is reduced and also power delay product is significantly reduced than the proposed design of (Keshavarzian et al., 2014).

Table-4 Simulation results with Frequency = 100MHz & Loads = 2fF (Keshavarzian et al., 2014)(Jafarzadehpour et al., 2015).

Properties	Power ($\times 10^{-6}$ W)	Delay ($\times 10^{-10}$ s)	PDP ($\times 10^{-15}$ J)
FA of (Ebrahimi et al., 2012)	6.361	2.838	1.806
FA of (Moaiyeri et al., 2011) first design	19.71	2.614	5.152
FA of (Moaiyeri et al., 2011) second design	1.462	3.861	0.564
FA of (Keshavarzian et al., 2014)	2.209	1.661	0.367
FA of (Jafarzadehpour et al., 2015)	0.182	2.635	0.48

In (Jafarzadehpour et al., 2015) ternary full adder is proposed which consist of two units of Ternary Half Sum Generator (THSG) circuit and one Carry Generation unit. In this an initial carry generation units are proposed this carry generation unit is modified in three stages to consume less power and to achieve better performance. Ternary full adder circuit is produced by modifying initial sum generation unit and with finally modified carry generation unit. This circuit when compared with the designs (Keshavarzian et al., 2014) achieves significant decrease in delay, less power consuming and also in PDP is significantly reduced.

In (Azimi et al., 2014) ternary multiplier circuit is proposed with analog multiplier so as to reduce the circuit size. Ternary inputs are converted to analog inputs by using transformer, after generation of product by analog multiplier this analog product is again converted to ternary output by using analog to ternary converter circuit. In the input side two ternary to analog converters are used. This multiplier circuit used as core multiplier is proposed in (Valle et al., 2001). The analog



inputs generated are multiplied on the multiplier and outputs are converted to ternary logic through converters. The number of transistors required by this design is quite less when compared to the multiplier presented in (Bachtold et al., 2001), due to reduction in number of transistors chip complexity and size of chip is reduced. In (Das et al., 2018) 1-bit ternary multiplier circuit is proposed by using four ternary multiplexer. Ternary multiplexer circuit consists of three pass transistors and three inverters. Two ternary decoder circuits are required in this circuit as two inputs are there. In this proposed design power consumption is less and delay is reduced when compared with the circuits presented in (Azimi et al., 2014)(Bachtold et al., 2001).

Table-5 Simulation results (Das et al., 2018).

Multiplier	Delay (sec)	Power in (W)
Multiplier (Valle et al., 2001)	2.6×10^{-7}	4.17×10^{-3}
Multiplier (Azimi et al., 2014)	66.8×10^{-9}	5.81×10^{-2}
Multiplier (Das et al., 2018)	32.4×10^{-12}	686.0×10^{-9}

V. CONCLUSION

In this paper Carbon Nanotube Field Effect Transistor (CNTFET) and ternary logic is briefly described at first, followed by CNTFET based logic circuits. Logic circuits of Half adder, Full adder and Multiplier are briefly reviewed. Simulation results shows that use of resistors as pull ups increases power consumption also the use of large resistors are undesirable. Therefore, CMOS design style is implemented in CNTFET to remove these large resistors. When binary and ternary logic are used together in a circuit it can significantly improve circuit performance and also consumes less power. Ternary logic lessens the numbers of interconnections and also chip area required is less, whereas binary logic is worthy for units that needs fast computing. Capacitors used in certain circuits leads to increase in power consumption and parasitic effect, therefore it is desirable to remove the capacitors to attain low power consuming and better performance of circuit.

VI. REFERENCE

[1] Vudadha, C., Katragadda, S. and Phaneendra, P. S. (2013). 2:1 Multiplexer based design for ternary logic circuits, 2013 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and

Electronics (PrimeAsia), Visakhapatnam, 2013, (pp. 46-51), doi: 10.1109/PrimeAsia.2013.6731176.

[2] Hurst, S.L. (1984). Multiple-Valued Logic—its Status and its Future. in IEEE Transactions on Computers, vol. C-33, no. 12, (pp. 1160-1179), Dec. 1984, doi: 10.1109/TC.1984.1676392.

[3] Dubrova, Elena. (1999). “Multiple-Valued Logic in VLSI: Challenges and Opportunities”. Proceedings of NORCHIP'99, 1999, (pp.340-350), doi:10.1.100.1809.

[4] Kim, Yong-Bin. (2010). Challenges for Nanoscale MOSFETs and Emerging Nanoelectronics. Transactions on Electrical and Electronic Materials, 11(3), (pp.93–105), doi:10.4313/TEEM.2010.11.3.093

[5] Iijima, S. (1991). Helical Microtubules of Graphitic Carbon. Nature, vol. 354, (pp.56-58), Nov 1991.

[6] Iijima, S. and Ichihashi, T. (1993). Single-shell carbon nanotubes of 1-nm diameter. Nature, vol. 363, (pp. 603-605), Jun 1993

[7] Stanford University CNFET Model website, <http://nano.stanford.edu/model.php?id=23>.

[8] Collins, Philip & Avouris, Phaedon. (2001). Nanotubes for Electronics. Scientific American. 283.62, Doi: 10.1038/scientificamerican1200-62.

[9] Das, D. , Banerjee, A. and Prasad, V. (2018). Design of ternary logic circuits using CNTFET. International Symposium on Devices, Circuits and Systems (ISDCS), Howrah, 2018, (pp. 1-6), doi: 10.1109/ISDCS.2018.8379661.

[10] Deng, J. and Wong, H. -. P. (2007). A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part I: Model of the Intrinsic Channel Region. In IEEE Transactions on Electron Devices, vol. 54, no. 12, (pp. 3186-3194), Dec. 2007, doi: 10.1109/TED.2007.909030.

[11] Deng, J. and Wong, H. -. P. (2007). A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part II: Full Device Model and Circuit Performance Benchmarking. In IEEE Transactions on Electron Devices, vol. 54, no. 12, (pp. 3195-3205), Dec. 2007, doi: 10.1109/TED.2007.909043.

[12] Raychowdhury, A. and Roy, K. (2005). Carbon-nanotube-based voltage-mode multiple-valued logic design. In IEEE Transactions on Nanotechnology, vol. 4, no. 2, (pp. 168-179), March 2005, doi: 10.1109/TNANO.2004.842068.

[13] Heung, A. and Mouftah, H. T. (1985). Depletion/Enhancement CMOS For a Low Power Family of Three-Valued Logic Circuits. Solid-State Circuits, IEEE Journal of. 20, (pp.609–616), doi: 10.1109/JSSC.1985.1052354



- [14] Lin, S., Kim, Y. and Lombardi, F. (2011). CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits. In IEEE Transactions on Nanotechnology, vol. 10, no. 2, (pp. 217-225), March 2011, doi: 10.1109/TNANO.2009.2036845.
- [15] Dhande, A. P. and Ingole, V. T. (2005). Design And Implementation Of 2 Bit Ternary ALU Slice. In Proceedings of International Conference IEEE-science of electronics, Technology of Information and Telecommunication, (pp. 17-21), Mar. 2005 .
- [16] Vudadha, C., Sreehari, V. and Srinivas, M. B. (2012). Multiplexer Based Design for Ternary Logic Circuits. PRIME 2012; 8th Conference on Ph.D. Research in Microelectronics & Electronics, Aachen, Germany, 2012, (pp. 1-4).
- [17] Ebrahimi, S., Keshavarzian, P., Sorouri, S. and Shahsavari, M. (2012). Low Power CNTFET- Based Ternary Full Adder Cell for Nanoelectronics. International Journal of Soft Computing and Engineering (IJSCE). 2231-2307.
- [18] Moaiyeri, M. H., Mirzaee, R. F., Navi, K., and Hashemipour, O. (2011). Efficient CNTFET-based Ternary Full Adder Cells for Nanoelectronics. Nano-Micro Letters. 3, doi: 10.5101/nml.v3i1.p43-50.
- [19] Keshavarzian, P. and Sarikhani, R. (2014). A novel CNTFET-based ternary full adder. Circuits, Systems, and Signal Processing, doi: 10.1007/s00034-013-9672-6.
- [20] Sahoo, S. K., Akhilesh, G. and Sahoo, R. (2017). Design of a High Performance Carry Generation Circuit for Ternary Full Adder Using CNTFET. 2017 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), Bhopal, 2017, (pp. 46-49), doi: 10.1109/iNIS.2017.19.
- [21] Jafarzadehpour, F. and keshavarzian, P. (2015). Low-power consumption ternary full adder based on CNTFET. IET Circuits, Devices & Systems, doi: 10.101049/iet-cds.2015.0264.
- [22] Azimi, N., Hosseini, H. and Shahsavari, A. (2014). Designing a Novel Ternary Multiplier Using CNTFET. International Journal of Modern Education and Computer Science 6, (pp. 45-51), doi: 10.5815/ijmecs.2014.11.06.
- [23] Valle, M. and Diotalevi, F. (2001). An analog CMOS four quadrant current-mode Multiplier for low power artificial neural networks implementation. ECCTD'01-European Conference on Circuit Theory and Design.
- [24] Bachtold, A., Hadley, P., Nakanishi, T. and Dekker, C. (2001). Logic Circuits with Carbon Nanotube Transistors. Science (New York, N.Y.). 294. (pp.1317-20), doi: 10.1126/science.1065824.

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