

IJEAST

INTERNATIONAL JOURNAL
OF ENGINEERING APPLIED SCIENCE
AND TECHNOLOGY

VOLUME : 2 ISSUE : 4 Print / Issue Publication Date: 31-Mar-2017

ISSN : 2455-2143

Indexed In

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International Journal of Engineering Applied Sciences and Technology, 2017
Vol. 2, Issue 4, ISSN No. 2455-2143, Pages 285-289
Published Online February-March 2017 in IJEAST (http://www.ijeast.com)



CASE STUDY OF 64-BIT LOW POWER PARALLEL PREFIX ADDER FOR HIGH SPEED ARITHMETIC CIRCUITS

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Abstract-- **The addition of two binary numbers is the basic and most often used arithmetic operation on microprocessors, digital signal processors and data processing application specific integrated circuits. Parallel prefix adder is a general technique for speeding up binary addition. This method implements logic functions which determine whether groups of bits will generate or propagate a carry. The proposed 64-bit adder is designed using four different types prefix cell operators, even-dot cells, odd-dot cells, even-semi-dot cells and odd-semi-dot cells; it offers robust adder solutions typically used for low power and high-performance design application needs. The comparison can be made with various input ranges of Parallel Prefix adders in terms power, number of transistor, number of nodes. Tanner EDA tool was used for simulating the parallel prefix adder designs in the 250nm technologies.**

Keywords--Low Power VLSI; Parallel Prefix Adder; dot operators; 64-bit Parallel Prefix Adder;

I. INTRODUCTION

The parallel adder is the most important element used in arithmetic operations of many processors. With the rising popularity of mobile devices, low power consumption and high performance integrated circuits has been the target of recent research. However, the two design criteria are often in conflict and that improving one particular aspect of the design constrains the other. Extends from the idea of carry look- ahead computation, a class of parallel carry look-ahead schemes are formed targeting at high-performance applications. A Parallel Prefix Adder (PPA) is equivalent to the CLA adder [2]. The two different in the way their carry generation block is implemented. The parallel prefix carry- look ahead adder was first proposed some twenty years ago as a means of accelerating *n*-bit addition in VLSI technology. It widely considered as the fastest adder and used for high performance arithmetic circuits in the industries. A three step process is generally involved in the construction of a Parallel Prefix Adder. The first step involves the creation of generate and propagate signals for the input operand bits. The second step involves the generation of carry signals. In the final step, the sum bits of the adder are generated with the propagate signals of the operand bits and the preceding stage carry bit using a xor gate. The figure 1 shows the three step process is generally involved in the construction of a Parallel Prefix Adder.

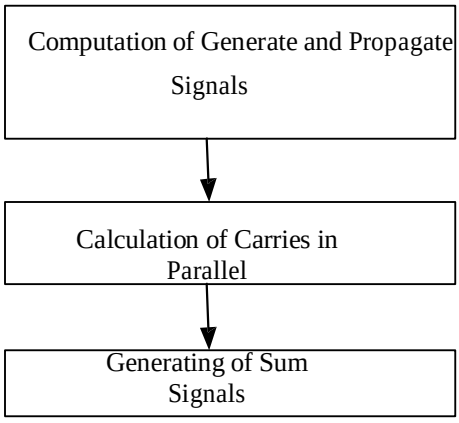


Figure 1. Steps in parallel prefix adder

II. EXISTING PARALLEL PREFIX ADDERS

The arrangement of the prefix network specifies the type of the PPA. The Prefix arrangement described by Haiku Zhu, Chung-Kuan Cheng and Ronald Graham, has the minimal depth for a known 'n' bit adder. Best logarithmic adder structures with a fan-out of two for minimizing the area-delay product is presented by Matthew Ziegler and Mircea Stan. The Sklansky adder presents a least depth prefix network at the cost of increased fan-out for certain computation nodes [8]. The algorithm invented by Kogge-Stone has both optimal depth and low fan-out but produces massively complex circuit realizations and also account for large number of interconnects [9]. Brent-Kung adder has the merit of minimal number of computation nodes, which yields in reduced area but structure has maximum depth

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which yields slight increase in latency when compared with other structures. The Han-Carlson adder combines Brent-Kung and Kogge-Stone structures to achieve a balance between logic depth and interconnect count. Knowles presented a class of logarithmic adders with minimum depth by allowing the fan-out to grow [4]. Ladner and Fischer proposed a general method to construct a prefix network with slightly higher depth when compared with Sklansky topology but achieved some merit by reducing the maximum fan-out for computation nodes in the critical path [6]. Sparse tree binary adder proposed by Yan Sun and et al., combines the benefits of prefix adder and carry save adder [3][10]. Integer Linear Programming method to build parallel prefix adders is proposed by Jainhau Liu and et al., The proposed Parallel Prefix adder for 64-bits has been proposed.

III. PREFIX OPERATORS

In the above equation, '•' operator is applied on two pairs of bits and. These bits represent generate and propagate signals used in addition [7]. The output of the operator is a new pair of bits which is again combined using a dot operator '•' or semi-dot operator '◦' with another pairs of bits. This procedural use of dot operator '•' and semi-dot operator '◦' creates a prefix tree network which ultimately ends in the generation of all carry signals. In the final step, the sum bits of the adder are generated with the propagate signals of the operand bits and the preceding stage carry bit using a xor gate. The semi-dot operator ' ◦ ' will be present as last computation node in each column of the prefix graph structures, where it is essential to compute only generate term, whose value is the carry generated from that bit to the succeeding bit.

$$(P_i,G_i) \bullet (P_{i-1},G_{i-1}) = (P_i.P_{i-1}, G_i+P_i.G_{i-1})$$
$$(P_i,G_i) \circ (P_{i-1},G_{i-1}) = (G_i+P_i.G_{i-1})$$

These two operators are divided into four types of different types prefix operators [5].

IV. PROPOSED 64-BIT PARALLEL PREFIX ADDER

A. 32-Bit Parallel Prefix Adder

Figure 2 shows the design of the proposed 32-bit parallel prefix adder. The objective is to eliminate the huge overlay between the prefix sub-terms being calculated. Hence the associate property of the dot operator is working to retain the number of computation nodes at a minimum [1]. The first stage of the computation is called as pre-processing. The first stage in the architectures of the 32-bit prefix adder involve the creation of generate and propagate signals for individual operand bits in active low format. The second stage in the prefix addition is termed as prefix computation. This stage is responsible for creation of group generates and groups propagate signals. The stages with odd indexes use odd-dot and odd-semi-dot cells where as the stages with even indexes use even-dot and even-semi-dot cells.

B. 64-Bit Parallel Prefix Adder

The Proposed 64-bit parallel prefix adder has ten stages of implementation. CMOS logic family will implement only inverting functions. Thus cascading odd cells and even cells alternatively gives the benefit of elimination of two inverters between them, if a dot or a semi-dot calculation node in an odd stage receives both of its input edges from any of the even stages and vice-versa. But it is essential to introduce two inverters in a path, if a dot or a semi-dot computation node in an even stage receives any of its edges from any of the even stages and vice-versa. From the prefix graph of the proposed structure shown in Figure 3 , we assume that there are only few reduction, since these inverters if not eliminated, would have contributed to significant amount of power dissipation due to switching.

The output of the odd-semi-dot cells gives the value of the carry signal in that corresponding bit position. The output of the even-semi-dot cell gives the complemented value of carry signal in that corresponding bit position.

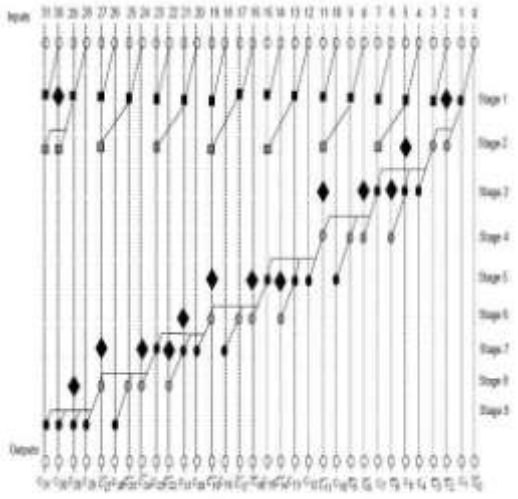


Figure 2. 32-Bit Parallel Prefix Adder

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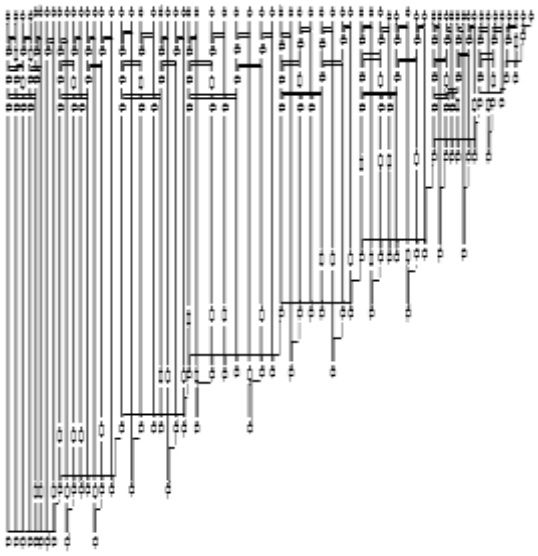


Figure 3. 64-Bit Proposed Parallel Prefix Adder

The final stage in the prefix addition is termed as post- processing. The final stage involves generation of sum bits edges with a pair of inverters, to make (G, P) as (G or to make (G , P) as (G, P) respectively. The pair of inverters in a path is represented by a in the prefix graph. By introducing two cells for dot operator and two cells for semi-dot operator, we have eliminated a large number of inverters. Due to inverter elimination in paths, the propagation delay in those paths would have reduced. Further we achieve a benefit in power bits and the carry bits generated in true form or complement form. The first stage and last stage are intrinsically fast because they involve only simple operations on signals local to each bit position. The intermediate stage embodies long distance propagation of carries, so the performance of the adder depends on the intermediate stage.

V. SIMULATION RESULTS

C. Proposed 64-Bit PPA

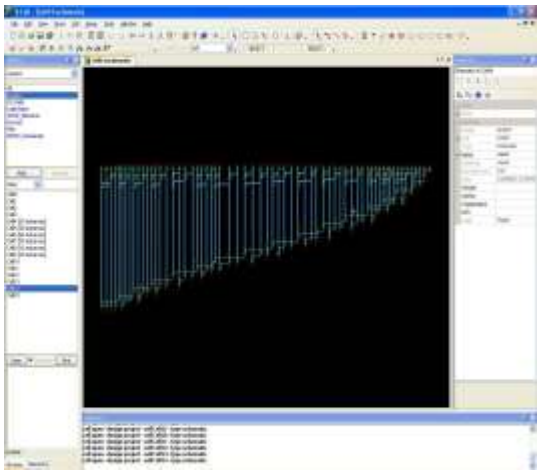


Figure 4. Block diagram for Proposed 64-Bit Parallel Prefix Adder

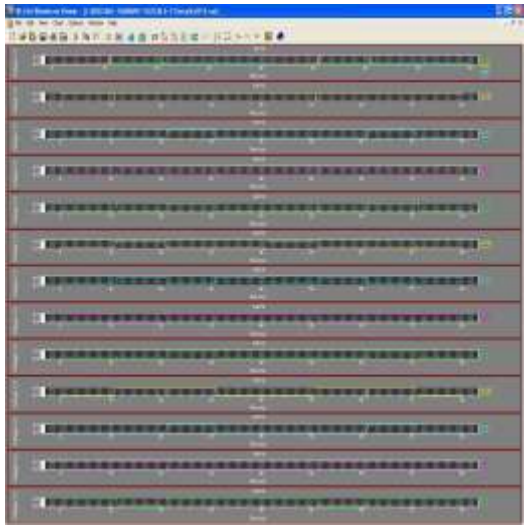


Figure 5. Output Waveform for Proposed 64-Bit Parallel Prefix Adder

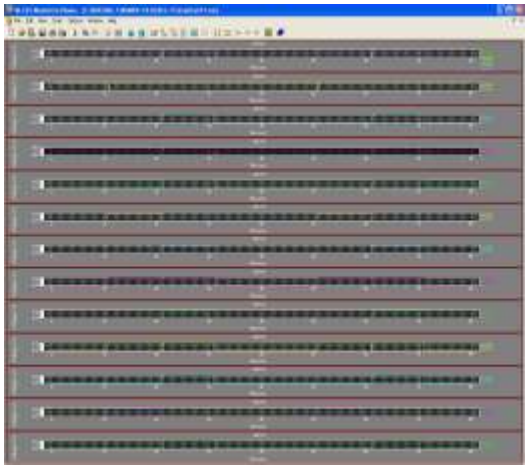


Figure 6. Output Waveform for Proposed 64-Bit Parallel Prefix Adder

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D. Comparison Charts

1) Power Comparison

The power comparison shows that, when number of input bits increased the power consumed by the adder will also increasing.

Table 1. POWER COMPARISION IN DIFFERENT VOLTAGE LEVEL

Adder	At V=5	At V=4	At V=3	At V=2
8-bit	4.45	2.51	.0090	0.002 4
16-bit	11.6	5.21	1.91	0.579
32-bit	20.0	8.82	3.03	0.804
64-bit	44.1	21.2	7.84	2.30

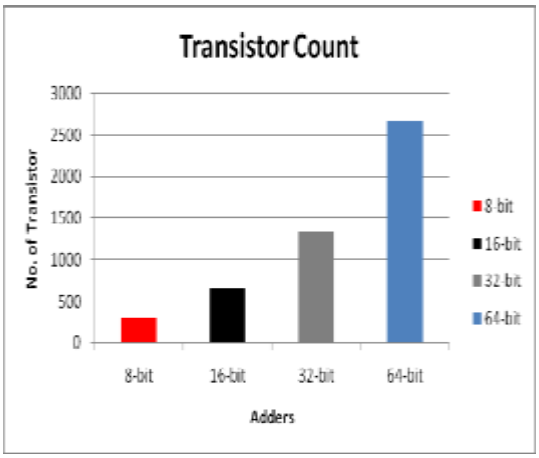


Figure 7. Power Comparison

2) Number of Nodes

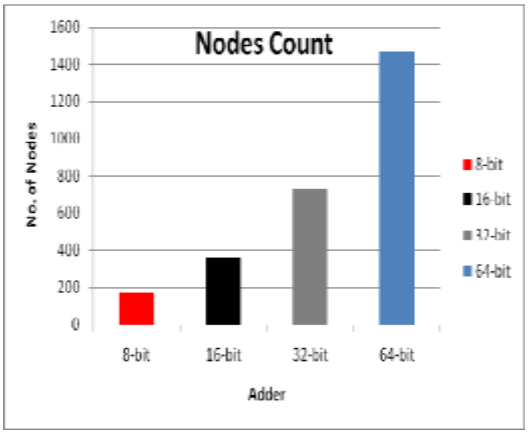


Figure 8. Number of Nodes*3) Number of Transistors*

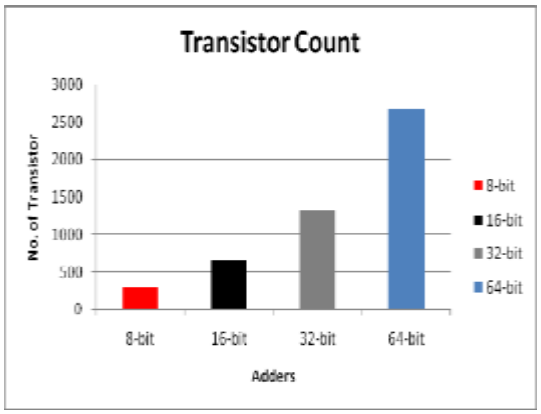


Figure 9. Number of Transistors

The above comparison graph shows the comparison of nodes and transistors in the 64-bit parallel prefix adder design.

VI. CONCLUSION

The parallel prefix formulation of binary addition is a very convenient way to formally describe an entire family of parallel binary adders. The proposed low power 64-bit parallel prefix adder were designed by using the four different prefix cell operators and compared with existing parallel prefix adders such as 8-bit PPA, 16-bit PPA, and 32-bit PPA. The performances in terms of Power, Number of nodes, Number of Transistor tradeoffs for various input ranges were analyzed. The power comparison can be made by varying the supply voltage from 1 to 5 for the entire parallel prefix adder designed. For 64-bit low power Parallel Prefix Adder Seventeen stages were used for generating the sixty three carries outputs and
1339 nodes were formed in the 64-bit low power Parallel Prefix Adder. The Proposed 64-bit low power prefix structure makes it more suited for Arithmetic Logic Units and multiplier units for complex ranges of input data computation. Tanner EDA tool was used for simulating the parallel prefix adder designs in the 250nm technologies.

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