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A LEAKAGE TOLERANT CMOS COMPARATOR

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Abstract—In digital VLSI design, domino logic style circuits are widely used. The domino of CMOS logic circuit dissipates very low standby power and exhibits less area. We design a comparator circuit which uses footed domino logic and also implement a current mirror circuit in the design, to enhance the speed of the comparator. Following paper emphasizes a proposed Comparator design which consumes low leakage power and had a higher speed, than other circuit. The delay, leakage power and average power of the proposed CMOS Comparator circuit have been calculated and simulated for high fan-ins (8, 16, 32 and 64 bits). The result shows a very small area overhead and 10%-30% reduction in total power dissipation. Also for some of the circuits, our circuit had a higher speed.

Keywords— Domino logic; leakage Power; delay; comparator; USDM

I. INTRODUCTION

Comparator is most important design element for various applications such as in processors of embedded, general purpose processor, DSP core, image / signal processing and built in self-test circuits [1]. Dissipation and minimization for the digital circuits requires optimization at all level of the design. So, this optimization depends on style of circuits topologies and in fact includes the technology which is used to implement the digital circuits [2]. The performance of the circuit can be enhanced by scaling MOSFETs to smaller dimension, which reduces the space complexity. The dimension normally refers to the channel length of the transistor. The key process that defines the minimum dimension in a technology, eventually led to channel length below 1 μ m, referred to submicron era. After this we had gone another scaling limit and below .35 μ m barrier, referred to Deep submicron (DSM) era. Scaling continued its relentless pace and then we entered a new era, where the minimum features of MOSFETs are being shifted to dimension below Deep submicron, so called Ultra Deep Submicron (USDM) technology [3]. The important challenges in this generation of IC designing is the increase in power dissipation in the circuit which reduces the battery – power, it is also effect the reliability of the circuit due to interconnect aging process and accelerated device.[4]. The major advantage of power analysis is the battery life of equipment is directly related to power dissipation [5]. Delay analysis also has important in synthesis of VLSI design. Integrated circuit designer have constantly sought accurate and

effect delay evaluation technique that will variety of option and better utilize the design space. There are different secondary effects like body bias effect, channel length modulation effect, velocity saturation effect, drain induced barrier lowering (DIBL) etc which will modify power and delay models. These secondary effects also put the limitations in the performance of the devices. The most popular delay model in DSM range is described Iⁿth power law. Where, velocity saturation is main consideration.

High fan-in comparators are widely used in circuit, such as high-performance microprocessor, communication system, and many other systems [6]. A faster and power efficient comparator is desirable. Superscalar microprocessors make extensive use of associative matching logic and comparators to support out-of-order execution and virtual memory mechanism. The traditional equality comparators used for implementing associative logic in modern data paths. Binary comparators are found in a wide variety of circuits, such as microprocessors, communication system, encryption devices, and many others. A faster, more power efficient, or more compact comparator would be an advantage in any of these circuits [7]

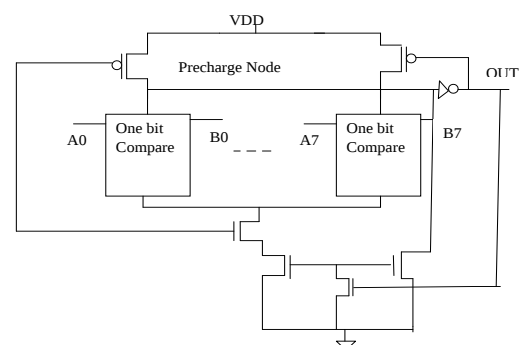


Fig 1: Block Diagram of CMOS Comparator

II. REVIOUS WORK

The schematic of a high fan-in (16-input) dynamic comparator based on standard footless domino logic comparator (FLDLC) has been shown in fig. In precharge mode, all inputs go low, and the precharge node is precharged high and the output goes low. During the precharge mode, CLK is low. So MP1 is on and MP2 is off. The precharge node started to charge high. The OUT node goes low and MP2 is turned on. Just when A

and B are different, the pull down transistors starts to discharging the precharge node, in the evaluation phase, when the clock is high, inputs are applied to the gate. If all corresponding bits of A and B inputs are equivalent;

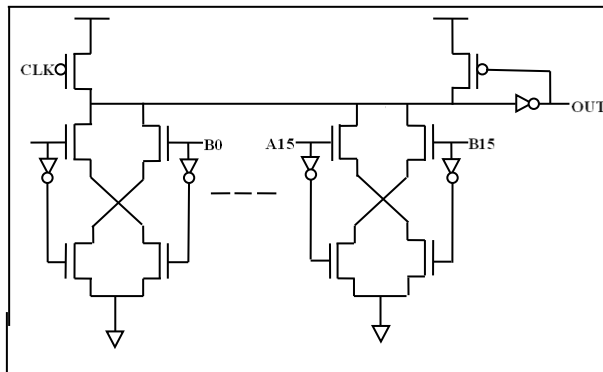


Fig 2: Footless Domino Logic Comparator

However if A and B inputs differ in any bit position, a conduction path from the precharge node to the ground is established, discharging the dynamic and causing the output to go high. Following figure describes about footless domino logic comparator.

A. A High Speed and Leakage Tolerant CMOS Comparator

Footed Domino logic comparator had been used in modern data paths (in applications alluded to earlier) where mismatches occur with a much higher frequency compared to full matches. Consequently, significant energy saving can be realized if comparators and associative logic can be designed to dissipate energy only on a full match and little or no mismatches. The domino logic comparator circuit's exhibit low leakage power also on the other hand FDLC circuit has lower speed than footless domino logic comparator circuit and also an overhead

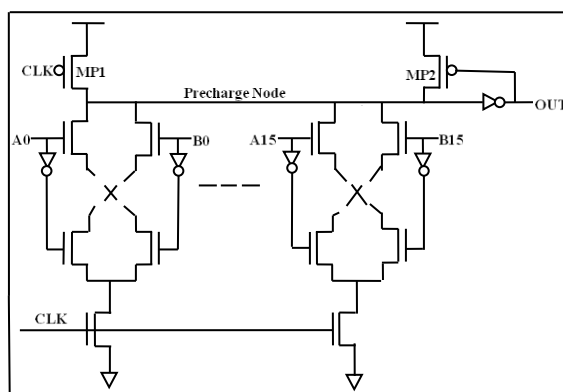


Fig 3: Footed Domino Logic Comparator

Another proposed circuit using pass logic, single stage comparator (PLSSC) , but this circuit has a lower speed than (FDLC) circuit which has its main problem. Further, FDLC comparator simulated circuit in 70nm CMOS predictive models. The power supply applied in the circuit was 0.9v due to which dissipate low power but it has low speed, which is overcome in the proposed comparator.

Thus Power and delay expression for the Domino logic comparator is as described as follows by:

The average consumption power of the circuit requires some input vectors to obtain accurate estimation the average power over the interval

In CMOS inverter circuit, three types of power dissipation occur.

A. Leakage power dissipation

When static current flows from VDD to ground node, without degrading inputs are called leakage power, the main components of leakage power in the OFF state at band to band tunneling, sub-threshold leakage (I_{sub}), and gate induced drain leakage, gate tunneling leakage.

Short circuit power

From α -power law [14], the short circuit power dissipation model is

Dynamic power dissipation

Dynamic power dissipation is associated with switching of transistor from high to low and low to high, i.e. due to the charging and discharging of load capacitances[15]

Where α is a switching activity factor of gate

Cl is a load capacitance.

Vdd is supply voltage

F is a operating clock frequency.

Therefore following Figure shows the schematic of our proposed Comparator. In this case only one of the evaluation branches conducts and discharges the pre-charge node. The worst case scenario for noise at the inputs is the case where all the inputs are low and receive the same noise in the evaluation phase. In the FLDLC, the keeper transistor is upsized from a keeper ratio of 1 to 2 in order to achieve different data points for delay and noise immunity. This circuit doesn't work fairly in high fan-in application. N-MOS Transistors M8 and M7 in our proposed circuit help evaluation phase to be faster. Because of using n-MOS transistors of minimum size, the evaluation phase will be slow without current mirror (M7, M8).

In our proposed circuit speed is almost independent of keeper size but we can achieve even more speed by increasing the size of NMOS transistor. Our simulation result is obtained in the case that is corner of the 45-nm CMOS technology at 0.7 V. Meanwhile the proposed circuit has better performance as compared to other domino logic circuit.

The FLDLC comparator fails to operate for smaller keeper sizes because of high leakage in scaled technologies. The

main problem of our circuit is dynamic power dissipation compared to PLSSC domino style circuit.

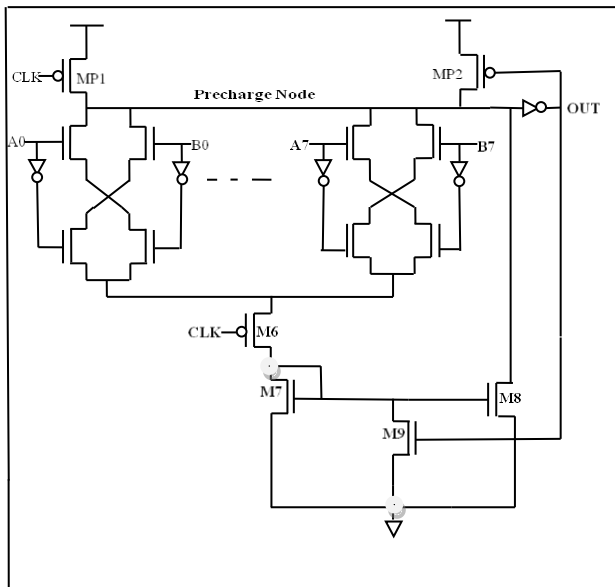


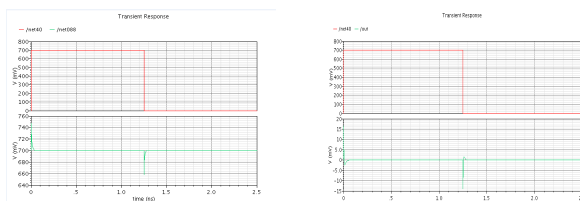
Fig 4: Schematic of CMOS Proposed Comparator

We compensate this power overhead using small size evaluation transistor and also low power supply voltage. The PLSSC circuit does not work properly in low supply voltage. Because charge sharing problem, does not let the output node to be in VDD voltage. Therefore figure shows that our proposed circuit has a smaller area compared with other circuits, because of employing minimum size evaluation transistor. Also in precharge phase four transistors consumes dynamic power that increases total power dissipation. The proposed circuit has a faster response time as compared with other circuits.

Following are the major contribution of the proposed comparators i.e. the various technique of power had been studied also various logic of CMOS magnitude comparator had been studied.

III. EXPERIMENT AND RESULT

In this paper a design of CMOS Comparator. The cadence virtuoso tool is used for estimating leakage power and average power consumption, is shown in table 1. Simulation results are taken with CMOS Technology, Supply Voltage = 0.7v, Pulse Width = 1.25ns, Delay time = 0ns, Rise time = fall time = 50fs. Simulation of CMOS Comparator is shown in both conditions: first when both inputs are same and second both inputs are different shown in Figure respectively.



(a) (b)

Figure 5 shows about the transient response of the circuit that relates the input and output waveform with respect to time in ns. From figure 6 it can be observed as delay, average power and leakage power increases as the no comparison increases. As shown, total power dissipation of proposed comparator is less than the other. These results are from low leakage in fan-in for the proposed comparator. The total power measured for 4, 8, 16, and 32 bits input with half bits matches. This metric is not exactly correct, but it can be an average of total power dissipation for different inputs.

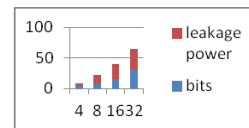
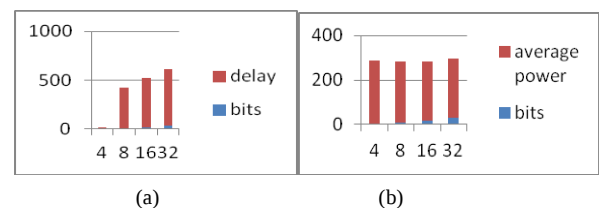


Fig 6: Delay, Average power and Leakage power comparison for CMOS logic Comparators

The main performances of our proposed CMOS Comparator are summarized in table 1. As shown the proposed CMOS Comparator achieves good performance characteristics in terms of Average power, Leakage power and Delay.

Table -1 Experiment Result

Bits	Delay	Average Power	Leakage Power
4	1.96ns	282.6mW	5.100pW
8	416.6ps	277.0mW	14.72pW
16	502.5ps	268.4mW	23.80pW
32	582.13ps	263.5mW	32.06pW

Table 1. Simulation Result of Proposed CMOS Comparator

IV. CONCLUSION

We have presented two designs for CMOS comparator



circuits that employed for low leakage and high speed applications. First circuit is a low power and high speed with very small area overhead. But about second circuit, is a low leakage, high speed and with no area overhead.

The Proposed Comparator for Ultra Deep Sub Micron range CMOS technology is suitable for high fan-in application. This proposed comparator circuit is optimal for low power, leakage tolerant and high speed application and found it suitable for high fan-in application. Also, the proposed circuit is power efficient for wide gates.

Cadence is used to verify the circuit performance. However, because of significant delay, it is a problem to maintain noise immunity in ultra deep sub micron technologies. We also count area for different circuits. The results show area of proposed circuit is smaller, because of employing minimum size evaluation transistor. Thus, the area counted by multiplies all W and L of transistors. Also in pre-charge phase four transistors Q6, Q7, Q8 and Q9 consumes dynamic power that increases total power dissipation. Hence proposed improved comparator using CMOS Logic style shows relatively large power savings over a range of supply voltage than the other comparators.

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