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DIGITAL CONTROL OF A CLOSED LOOP BUCK CONVERTER

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Abstract— **The primary focus for the R&D in this area so far has been to figure out the best approach for evaluating and designing the DC-DC converter and perhaps the most appropriate control technique is being applied in different DC-DC converter circuits. Depending on power handling capacity as well as high-frequency switching, certain switching devices are chosen. This paper discusses the deployment of the digital PID controllers in the DC-DC converters. In an attempt to get a quicker response, voltage mode control has been used. Digital controllers started replacing traditional analog controllers more and more. Better immunity to changes in the environment which includes temperature and degradation of components, improved versatility by modifying the software, increasing advanced control methods, and decreased number of the components are the key benefits of the digital control against the analog control. A structured and concise strategy for designing a digitally operated close-loop Dc / Dc buck converter is discussed in this paper beginning with the Buck converter and giving the set of certain performance specification, implementations of the digital Proportional-Integral-Derivative(PID) controller is made. It addresses in depth all the appropriate DSP hardware and/or software methods and approaches needed to implement a controller. In order to illustrate the efficacy of the model, the dynamic response as well as the steady-state performance of controller is provided. The experimental outcomes fit well with the model of simulation. During the implementations of Switch Mode Power Supply (SMPS), application of dsPIC provides new perspectives towards affordable and versatile approaches of digital control.**

Keywords— **DC-DC Converter, Buck Converter, Closed-Loop Control, Voltage Mode Control, Pulse Width Modulation, PID controller, Digital Control, Matlab/Simulink ®**

I. INTRODUCTION

In today's progressing information society, for applications such as communication and information processing, the contribution of power supply is becoming more and more important as the main part of the electronic communication tools. A DC-DC Converter is implemented to step-up or step-down a DC voltage level. The concept of a DC-DC converter is to switch the DC supply at high frequency, which in turn charges and discharges the inductor into the load following the required output voltage. These converters possess a switch-mode or a linear regulator. Linear converters contain a transistor in series operating in the active region. Thus, to adjust the output, it imitates a variable resistor. The limitation of a linear converter is that its conduction losses are high, due to which there is a reduction in efficiency. Alternatively, switch-mode converters have decreased conduction losses, however, there is an increase in switching losses. Hence, because of high frequency switching, high electromagnetic interference is produced. Switching power supplies are much more efficient and provide more power density as compared to linear power supplies. Energy storage elements, such as capacitors and inductors, are implemented for energy transfer and acts as a low-pass filter. The two intrinsic circuit topologies of a switch-mode DC-DC converter are boost and buck converters. Almost all of the other circuit topologies are either boost-derived or buck-derived since their topologies are identical to the boost or buck converters.

Conventionally, analog control techniques have been utilized to regulate the output of the DC-DC converters. Analog control systems have wide bandwidth and function in real time. Moreover, for analog systems, the voltage resolution is hypothetically infinite. There are two main advantages of analog systems: wide control bandwidth and economical. However, a large amount of complicated circuit hardware is needed for sophisticated control algorithms. Although, an analog system consists of separate hardware that needs to be changed to modify controller gains or algorithms. Additionally, the utilization of enhanced control algorithms needs an excess amount of component parts.

Diversely, the complication of digital control systems mostly involves in the software. Once it is operating functionally, the software is much more compatible and dependable compared to a complicated analog system. Breakthroughs in signal processing technology have prompted research in advance control techniques to enhance converter control. In recent years, digitally controlled DC-DC converters with the help of microcontrollers and DSPs have been made possible due to the

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advancement in technology in very-large-scale-integration (VLSI).

In addition, digital control continues to become a strong candidate in the oncoming generation of power supplies for the switch-mode because of both accelerated reductions in prices and rise in performance of digital signal processors (DSP) and microcontrollers. DC-DC converter with digital control offer many advantages over analog control.

1. More enhanced control algorithms, for instance non-linear and adaptive control can be implemented utilizing digital control.

2. Execution of digital control is more adaptable by modifying the software.

3. Power efficiency can be optimized by digital control.

4. Digital control can incorporate power management operations, for instance thermal management into a single digital control chip, effectively eliminating need of external components.

5. DC-DC converters implementing digital control have higher immunity to external changes, for instance aging of components and temperature.

Utilization of digital signal processors (DSPs), digital integrated circuits (IC) and microcontrollers can attain digital control of DC-DC converters. Digital signal processing (DSP) has found many applications in intelligent control, telecommunications, motion control, etc. Digital control utilizing DSP is becoming increasingly common in industries today due to its high reliability, high speed computation ability, and cost reduction. Normally, digital signal processors (DSP) have higher computational power as compared to microcontrollers. Consequently, a digital signal processor (DSP) is used to implement more advanced control algorithms. Contrarily, microcontrollers are cheaper than DSPs, thus providing solutions to digital control at a lower cost. This paper will be concentrated on the implementation of digital controllers employing digital signal processors (DSP).

Technological advances have given digital signal processors (DSP) and microcontrollers the requisite on-board functions to permit administration of a digital controller employing only one chip. An ADC (analog-to-digital converter) computes the output voltage and transforms it into a binary number correspondingly. Utilizing an algorithm from the memory storage, an additional duty cycle is determined by the control processing unit (CPU) and passes it to a pulse-width-modulation (PWM) module which regulates the primary switch in the converter. It takes a limited period of time to determine the output voltage, measure the new duty cycle, and modify the duty cycle, so that a digital controller implemented in a DC-DC converter has an inherent time delay. Additionally, most DSPs and microcontrollers only permit a new duty cycle to begin at the start of the following switching cycle once its computation is done. As a consequence, for the digital controller, the minimum time delay is equivalent to a unit converter switching cycle. In short, a control system's purpose is to make a physical system perform in the required way, allowing its output to track a predetermined reference input regardless of the presence of errors, disturbances and noise in the modelling. The controller, which produces the necessary control signal for physical system operation, is one of the key elements of a control system. [2]

This paper introduces to the step-by-step design of digital control employing a DSP and its implementation in a DC-DC converter. It explores all the requisite DSP software or hardware techniques and algorithms needed to implement the controller, beginning with a dc-dc buck converter and a given set of design specifications, such that it can be implemented easily by engineers. We propose to design a buck converter employing a PID controller in MATLAB. While the input voltage and load varies rapidly, the fluctuation peak of the output voltage is minute. This results in shorter recovery time due to its fast recovery towards reference voltage. Eventually, the dynamic operation of a DC-DC buck converter can be improved by this method. However, this paper still focuses primarily on implementing a simple solution which is easily adaptable in the design of a PID controller for DC-DC buck converter, to narrow the gap between the theoretical principle of control and its circuit implementation. On the other hand, the solution is described in a way that includes only a basic digital PID based buck converter model and simple directed steps and equations for design. Hence, when designing the controller, the designer can be allowed to skip through the tedious initial derivations.

Section 1 introduces to the basic principles of the digital control of a closed loop buck converter. The basic description of a buck converter and its design parameters are discussed in section 2. Sections 3 and 4 describe the open and closed loop mode of a buck converter respectively, and their design values, along with their simulation models. The digital blocks of the DSP based PID controller are explained individually in section 5. Section 6 gives a detailed representation of the design process of the digital controller implemented in the DC-DC buck converter, its digital sampling loop implementation and circuit configuration. Sections 7 and 8 gives a brief report of the simulation and experimental results with graphs. To conclude this paper, the experimental results and the simulation results are compared.

II. BUCK CONVERTER

A Buck converter is a type of switch mode DC to DC power converter in which the output voltage is transformed to level

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less than the input voltage. A Buck Converter also known as a step-down converter. The name step down converter is based on the fact that it is analogous to step down transformer where the input voltage is bucked (stepped) down to a level less than the input voltage. The DC input required can be obtained from the AC mains (line) via a rectifier/reservoir capacitor circuit or from any DC supply. If the input is a DC supply, then electrical isolation between the switching circuit and the output is not required. Whereas the isolation could be provided if the input is obtained by the rectification of the AC input supply between the AC source and the rectifier using a mains isolating transformer. The AC input given to the rectifier circuit could be either AC at high voltage which is obtained directly from the AC mains supply, or a lower voltage attained via a step-down transformer. Nevertheless, the derived DC voltage of the buck converter is converted to an AC voltage with high frequency, using a switching transistor, which is driven by a PWM square wave. This results in an AC wave with high frequency, which can be again converted into a DC voltage more efficiently. Buck Converter mainly consists of semiconductor switches such as MOSFET, IGBT, diode and passive elements like inductors, capacitors, resistors. The switching transistor of the buck converter, situated between the input and output, continually switches ON and OFF at high frequency. The switching of Semiconductor Switches is controlled by gating signal (q). When the value of q is high (1), MOSFET is in on state and when the value of q is low (0), MOSFET is in off state. The circuit of the buck converter uses the energy collected in the inductor L, to continue supplying the load during the OFF periods. This energy is stored during the ON stage of the switching transistor to maintain continuous conduction of the buck converter. A schematic diagram of a Buck converter which has same polarities on both input and output voltages is shown in Figure.

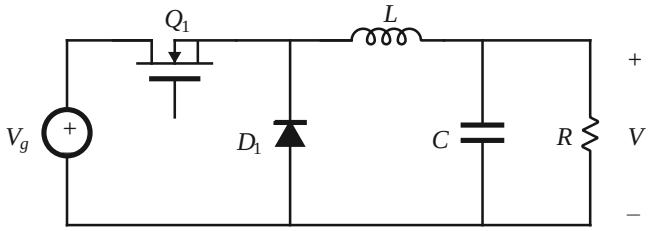

Fig. 1. Buck Converter

A. Design Parameters –

A Buck Converter with input voltage Vg and output voltage V its duty cycle D can be determined as follows:

$$D = \frac{V}{Vg} \tag{1}$$

Basic Design of Inductor: Increase in the value of the inductor increases the maximum output current due to the decreased ripple current. The lower the value of the inductor, the smaller the size of the solution would be. Remember that since the current rises with reducing inductance, the current rating of the inductor must always be much more compared to the maximum current. For quantities where the range of inductor is not given, a reasonable approximation for the right inductor can be done as per (2). The inductor's minimum value shall be computed from,

$$L = \frac{V\left(V_g - V\right)}{\left(\Delta i_L \times F_s \times V_g\right)} \tag{2}$$

Where:
Vg: Input voltage.
Δi_L: Inductor ripple current.
V: Output voltage.
F_s : Switching Frequency.

Basic Design of Capacitor: Best approach would be to utilize low Electrolytic series resistor (ESR) capacitors to reduce the ripple voltage upon its output side. If a converter has external compensation, any value of the capacitor more than its suggested minimum in the data sheet could be implemented, but the compensation has to be modified for the utilized output capacitance. The specified capacitor and inductor values must be employed for internally compensated converters or else the instructions in the data sheet for modifying the output capacitors for the implementation should go along with the L × C ratio. The following Equation (3) could be used with external compensation to change the values of the output capacitor for an intended ripple in the output voltage. At 1 per cent or less of V_{out} variations, the minimum value of a capacitor value is given as:

$$C = \frac{\Delta i_L}{8 \times F_s \times \Delta V_c} \tag{3}$$

Where:
Δv_L: Output Ripple Voltage.
Δi_L: Inductor ripple current.
F_s: Switching Frequency.
Basic Selection of Diodes: Fast recovery diodes are preferred as they have diffusion junction, lower forward voltage drop, and high current capacity with high efficiency. The average current of the diode must be greater than that of the DC / DC converter's peak inductor current. The reverse breakdown voltage of the diode should be higher than the maximum buck-circuit input voltage. Schottky diodes are implemented to minimize losses. The required forward current rating is equivalent to the maximum current of the output:

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$I_f = I_{out(max)}$ (4)

Where:
I_f : Average forward current of the rectifier diode.
$I_{out(max)}$: Maximum output current.

Schottky diodes possess higher peak current rating compared to the average rating. The elevated peak current of the system is not really a concern. The power dissipation of the diode is the other parameter that has to be tested. Power Dissipation of the diode can be calculated by,

$$P_D = V_F \times I_F \quad (5)$$

Where:
I_f: Average forward current of the rectifier diode.
V_f: Maximum output current.

III. CLOSED-LOOP CONTROL OF BUCK CONVERTER

In the closed-loop control, the buck converter is operated in DCM, which stands for discontinuous conduction mode. It is regulated by a PID controller and a PWM controller in voltage-mode. A closed-loop buck converter is used to acquire a steady DC output voltage. The DC output voltage is regulated by the switching frequency as well as the duty cycle. The reference voltage is juxtaposed with the output voltage in the closed-loop method, and by regulating the switching pulse, the error value is brought to a minimum. The basic concept behind the closed-loop converter operation is that if a positive error value is obtained, the duty cycle is minimized and the duty cycle is increased if the negative value of error is obtained. The output voltage is kept constant by continuing the process ceaselessly. In this scheme of closed loops, Fig. 2., the first voltage required was set to V_{ref}. The calculated output voltage V is the feedback and the error detector was used to compare both Vref and V and the produced error was fed to the PID controller to take PID control action. We also outlined the error correction of the PID controller and the duty cycle computation in simulation to produce PWM, which is further contrasted with the saw tooth waveform. The output of PID controllers is taken as δ(t). To have the final current reference, all reference currents are again summarized and averaged. Since we need automated duty cycle generation, we do not explicitly use the pulse generator. In contrast to the open-loop method, the closed- loop method gives us a more precise result. The controller modifies and tries to manipulate the actuating signal in closed-loop systems in such a manner that the system error is zero. The system detects changes in the environment, as well as internal disturbances. So, the precision of such a system is often very high.

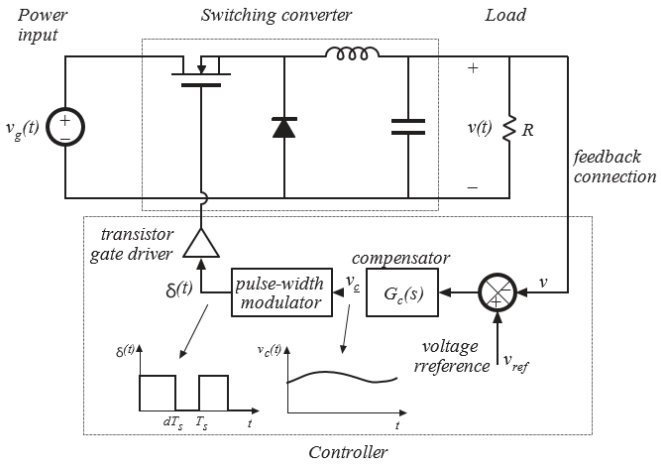

Fig. 2. Closed Loop control of a Buck Converter

A. PID Controller –

Proportional Term: The Proportional controller drives the position to zero.

$$u(t) = K_p \times e(t) \quad (6)$$

where e(t) is the error at time t and K_p is proportional gain. A block diagram of a P controller implemented to control a system is shown in Fig. 3

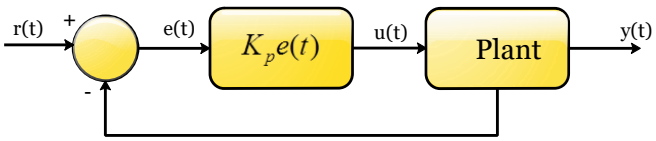

Fig. 3. Block Diagram of Proportional Controller.

The proportional gain Kp acts as a 'software-defined spring' that pulls the system at a desired position. As studied in physics, if we produce a model of spring as F = −kx, where k is the proportional constant, x is the displacement and F is the applied force. The above equation can also be written as F = k (0 − x) where 0 is the equilibrium point. The equation could have a one: one correspondence if the set point of the feedback controller is kept equal to the equilibrium point.

$$F = k(r - x) \quad (7)$$

$$u(t) = K_p e(t) = K_p\left(r(t) - y(t)\right) \quad (8)$$

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Thus, the force applied on the system's output by the proportional controller to pull it toward the set point is directly proportional to the error of the system.

Integral Term: The Integral controller accumulates the area between the output and the set point plots over a period of time (in other words, the integral of position error) and adds the total current to the control input. The accumulation of the area between two curves is known as integration.

$$u(t) = K_p e(t) + K_i \int_0^t e(\tau) d\tau \tag{9}$$

Where Ki is integral gain, Kp is proportional gain, T is integration variable and e(t) is the error at time t. The integral controller integrates starting from time 0 to time t. In the steady-state, when the system is close to the set point, the proportional controller is too small to pull the output to the desired set point, and the derivative term becomes zero. This results in a steady state error. A common solution to eliminate steady-state error is to integrate the error and then add the integrated value of the error to the control input. Because of this, until the system converges, the control effort increases.

The Fig. 4 below is a block diagram of a PI controller controlling a system.

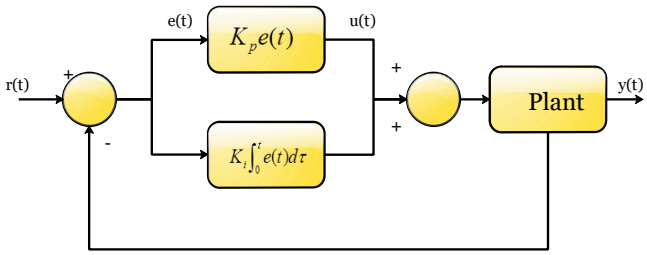

Fig. 4. Block Diagram of Proportional- Integral Controller.

Derivative Term: The derivative controller drives the error value of velocity to zero.

$$u(t) = K_p e(t) + K_d \frac{de}{dt} \tag{10}$$

Here K_p, K_d are the proportional and derivative term respectively. The Fig. 5 is a block diagram of a PD controller controlling a system. A PD controller consists of Kp and Kd, which are

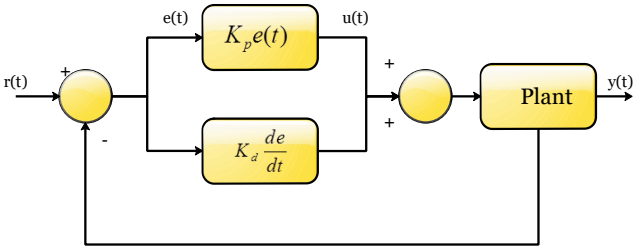

Fig. 5. Block Diagram of Proportional- derivative Controller

the proportional controllers for position and velocity respectively. Change in position set point over time provides the set point for the velocity. To prove this point, we have rearranged the PD controller equation.

$$u_k = K_p(r_k - x_k) + K_d \frac{(r_k - x_k) - (r_{k-1} - x_{k-1})}{dt} \tag{11}$$

$$u_k = K_p(r_k - x_k) + K_d \frac{r_k - x_k - r_{k-1} + x_{k-1}}{dt} \tag{12}$$

$$u_k = K_p(r_k - x_k) + K_d \frac{r_k - r_{k-1} - x_k + x_{k-1}}{dt} \tag{13}$$

$$u_k = K_p(r_k - x_k) + K_d \frac{(r_k - r_{k-1}) - (x_k - x_{k-1})}{dt} \tag{14}$$

$$u_k = K_p(r_k - x_k) + K_d \left(\frac{r_k - r_{k-1}}{dt} - \frac{x_k - x_{k-1}}{dt} \right) \tag{15}$$

Notice that the $\frac{r_k - r_{k-1}}{dt}$ is the velocity set point. Similarly, $\frac{x_k - x_{k-1}}{dt}$ is the velocity of the system at a determined time step. This means that the estimated velocity is being driven to the set point. velocity by the term K_d of the PD controller. The absolute velocity set point is null if the set point is kept constant. Hence, if the system is moving, the term K_d slows it down. This imitates a 'software-defined damper'. These has mainly found application in door closers, and its damping force rises linearly with velocity.

PID Controller: When the above three terms are combined, we get the definition equation of a PID controller.

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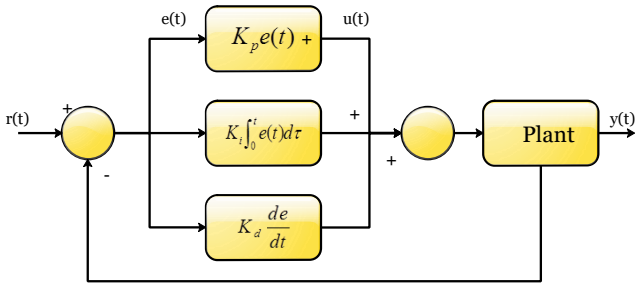

Fig. 6. Block Diagram Of PID Controller.

IV. MODELING A DIGITAL CONTROLLER.

The quickest method of accomplishing digital control is to design the system in the analog discipline and then transfer it to its equivalent in the digital domain. Feedback quantization, disturbances latency response and the delay necessary to calculate the error & sample the feedback, should be considered if the model has an analog control base.

The Fig. 7 shows the block diagram of closed-loop DC/DC buck converter employing average current mode control.

The blocks I_{sense} and V_{sense} measure the output current and voltage through the inductor. The above measured values act as inputs for the ADC (analog to digital converter). The changed output voltage V[t] is subtracted from the predetermined reference voltage Vref to obtain the error value eV [t] in the voltage loop. The value executed in the software is $V_{ref.}$ The $G_c v(z)$ compensator block takes the error eV [t] as its input.

The current loop reference, I_{ref}, is the output obtained from this block. The converted inductor current, I [t], is subtracted from the reference current, I_{ref}, to obtain the input for the block $G_c i$ (z). The output obtained from the second compensator $G_c i$ (z) sets the digital pulse width modulation (DPWM) value.

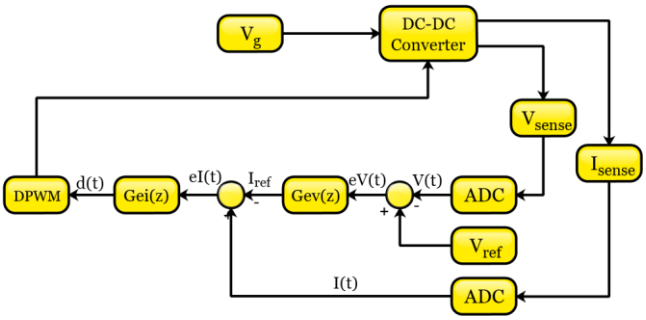

Fig. 7. Block Diagram Of Close-Loop

According to power converter specifications, employing different parameters for the passive components, the analog controller has to be re-modelled and implemented. The passive components used in the analog controller are vulnerable to environmental conditions. To secure a stable loop in all performing conditions, the components' tolerance should be low enough.

The compensation variables in digital controllers can be converted with no necessary alteration to the hardware. Compared to passive components, digital processors are less vulnerable to external conditions. The benefits that digital control has over analog control are the incorporation of more control features in the processor and the repeatability of the control algorithms.

The transfer functions in the s-domain are converted into z-domain while executing a digital controller based on its analog counterpart. To make the system stable, the poles and zeroes are computed. Once this is done, the digital transfer function coefficients in the z-domain are easily found using MATLAB. Because of this, the power supply compensation of both analog and digital controllers are alike. A fixed-point digital signal processor is employed in place of a floating-point digital signal processor for low cost applications. Due to the quantization elements which exist in the digital control loop, a digital controller has a defined set of distinct values. Once per switching sequence, the controller function is called. In the worst case, the controller will sense a disturbance with one switching cycle delay. Two registers are used to generate the duty cycle. One register defines the duty cycle period and the other stores the duty cycle value.

Due to the increase in slew rate of the operational amplifier and the continuous sampling of the analog environment, the analog control responds instantly to disturbances. Comparison of the error voltage with the saw tooth signal provides the duty cycle. It is important to research the significant blocks in the architecture of digital control to better understand the distinctions between digital and analog controllers. Analog to digital converter (ADC) is the first component that influences the digital controller's output.

4.1. An Analog to Digital Converter(ADC).

The resolution of the Analog to digital converter (ADC), determines the accuracy with which Vout is regulated by the digital controller.

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$$resolution_{ADC} = \frac{V_{ref}}{2^n}\left[\frac{V}{LSB}\right] \quad (16)$$

where Vref represents the reference voltage of the converter and in the number of bits. The resolution of the output voltage set by the system is defined by the resolution of the analog to digital converter. The accuracy and gain of the external resistive divider are necessary to be taken into consideration to determine the actual measurement resolution.

The time needed between the command that initiates the sampling and when the result becomes available in the output register of the ADC is of great importance. Another aspect is related to bandwidth of the control loop. This latency limits the operating frequency of the duty cycle. Because the conversion time can be considered a delay, the digital controllers cannot have the instantaneous reaction of the analog controllers. The values converted by the ADC are saved in the memory of the controller and used for calculating the duty cycle.

4.2. Digital Pulse Width Modulation(DPWM).

If the resolution is not sufficient enough, the digital pulse width modulation (DPWM) generates unwanted oscillations. In a digital controller, the pulse width has a defined number of discrete values and equation for the resolution is given below:

$$N = \log_2\left(\frac{F_{clk}}{F_{sw}}\right)[bits] \quad (17)$$

There is a chance of limit cycle oscillations occurring if the resolution of the DPWM is not high enough.

4.3. Limit cycling.

Due to unavailability of DPWM level, the controller will alternate around the zero-error value. In an ideal state, it will try to drive the Vout to zero error. Output voltage variation is large which may be due to limited cycling in steady-state. To overcome this effect, the DPWM's resolution has to be smaller than the ADC resolution. Assurance of small difference of resolution results in 2 DPWM levels per 1 level of ADC. Dithering is one way to improve the effective resolution of DPWM. Digital dither can be created inside the controller which is easy to apply and control. This can provide more flexibility. A soft start needs to be provided when a controller is used for power supply.

4.4. Soft Start

The inrush current at the start-up is avoided by the soft start function. The techniques are referred to as open-loop soft start since the regulation loop opens throughout the soft start. The duty cycle increases with the slow increase of the soft-start capacitor voltage until the duty cycle obtains a nominal value.
It is easier to execute this logic in a digital controller. A small quantity is added to the duty cycle register until the required output voltage is attained. The algorithm for the closed-loop starts after this procedure. The block diagram of a digital controller implementing the above mentioned functions is shown in Fig. 8.

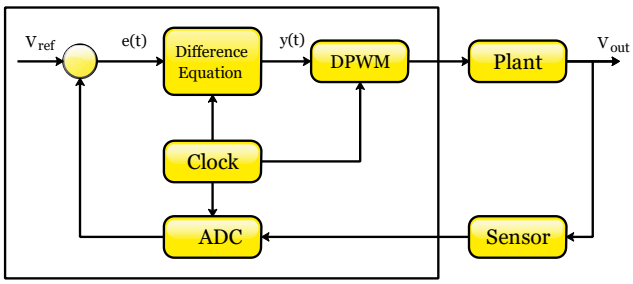

Fig. 8. Block Diagram Of Standard Digital Control

V. Digital Control of a Closed-Loop Buck Converter

A DSP-based proportional-integral-derivative (PID) controller implementation of a buck converter is shown in Fig. It should be noted that, the compensator, pulse width modulator (PWM) and voltage sensing operations are still there in the system based on DSP; however they occupy different names. The voltage divider circuit supply the feedback sensing system to the Converter, like in the conventional methods.

5.1. Configuration of Digital PID Controller.

The typical process of designing the digital controller of the buck converter consists of methods to overcome the converter's weak points, for instance, at low frequency, the DC gain is low and at high frequency, the phase margin is poor. Thus, at this stage and with the help of the table, it becomes possible to model a DC-DC buck converter with the standard method, emphasising on the weak points and enhancing its parameters by the implementation of a PID controller. Our description below begins with the supposition that the parameters of the buck converter are realized and they are given in the Table 1.

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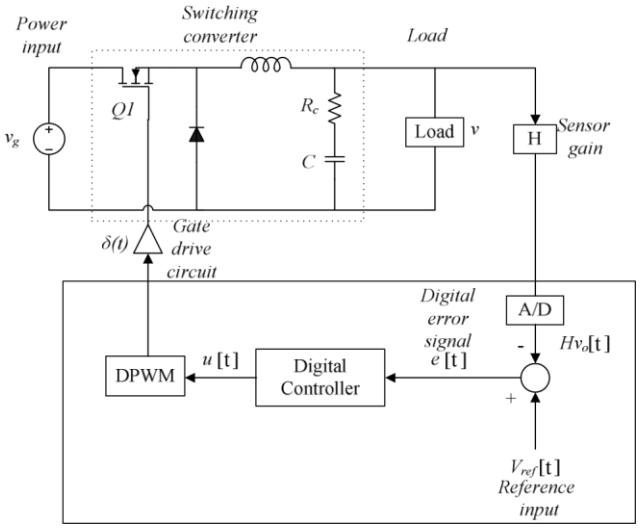

Fig. 9. Circuit Diagram Of Digitally Controlled Buck Converter

Table 1
Buck Converter Design Parameters.

Parameters	Values
Input Voltage, V_g	458V
Output Voltage, V	200V
Switching Frequency, F_s	25kHz
Inductance, L	1.5021mH
Capacitance, C	0.1875μF
Output Current, I_o	10A
Resistance, R	12Ω

5.1.1. Method of Tuning PID Controller.

Two main conditions should be satisfied by the loop transfer function:

1. The transfer function should not include any right pole and it has to be proper.

2. The negative semi-real axis and the unit circle should be intersected by the polar plot of L(jω) for ω > 0 only once.

If this specification is fulfilled, then move toward the method discussed below.

Transfer function of Proportional-Integral-Derivative controller:

$$C_{PID} = K_P\left(1+\frac{1}{T_i s}+T_d s\right) \tag{18}$$

Equation (19) in its polar form can be written as

$$C_{PID}(j\omega) = M(\omega)e^{j\Phi(\omega)} \tag{19}$$

In Continuous Conduction Mode the plant of the Buck converter is given by:

$$\frac{v_o}{d} = \frac{V_{in}}{LC}\frac{1+srC}{s^2+s\left(\frac{1}{RC}+\frac{r}{L}\right)+\frac{1}{LC}} \tag{20}$$

The plant contains one zero and one pair of complex poles. To design the digital controller, we have to calculate the pole, zero and gain for a specified bandwidth.

If fc = 25kHz and Øm = 60◦.

$$G_C(s) = \frac{k}{s}\frac{\left(1+\frac{s}{\omega_z}\right)^2}{\left(1+\frac{s}{\omega_p}\right)^2} \tag{21}$$

In the plant phase gain must be measured at the appropriate bandwidth.

$$\left|G_P(s)\right|_{s=j\omega} \tag{22}$$

$$\phi_{boost} = -90^\circ + \phi_{PM} - \angle G_P(s)\big|_{s=j\omega} \tag{23}$$

$$k_{boost} = \tan\left(45^\circ + \frac{\phi_{boost}}{4}\right) \tag{24}$$

$$k = \frac{1}{\left|G_P(s)\right|_{s=j\omega}} \tag{25}$$

$$\omega_z = \frac{2\pi f_c}{k_{boost}} \tag{26}$$

$$\omega_p = 2\pi f_c k_{boost} \tag{27}$$

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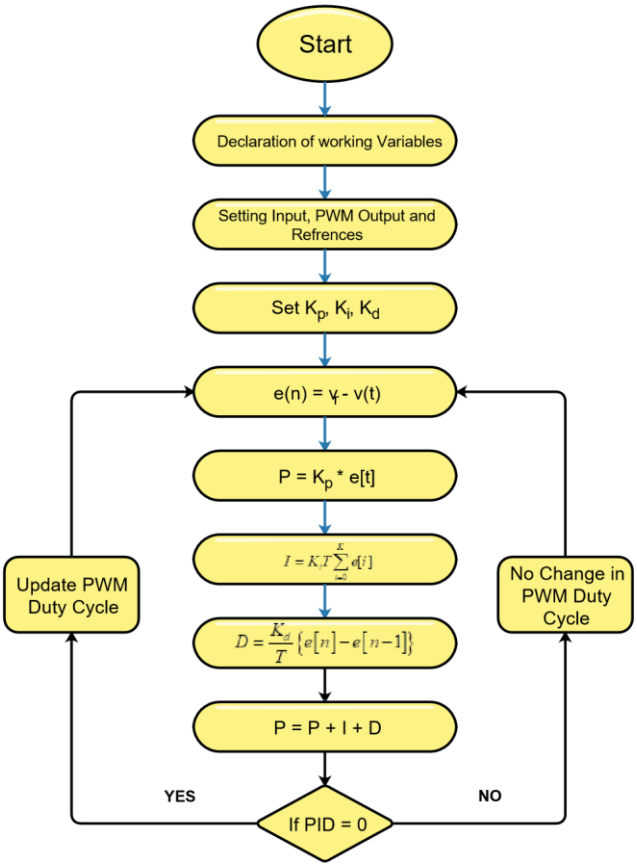

Fig. 10. Block Diagram Of PID Controller

5.1.2. Validation of the procedure outlined above.

The method described above is applied to Buck regulator to check if the parameter values that are received from the buck regulator from the previous approach offers or does not give a suitable outcome. The code required for tuning the PID controller, done in MATLAB is shown below.

MATLAB Command Window Page 1

```
>> s = tf('s'); G = 1/(s+1); options =
bodeoptions('cstprefs'); options.FreqUnits =
'Hz'; % or 'rad/second', 'rpm', etc.
bode(G,opti
ons); Vin =
458;
L = 1.5021e-3;
C = 0.1875e-6; R= 20; r= 1; Gps = Vin/(L*C) *
(1+s*C*r)/ (s^2 + s*(r/L + 1/(R*C)) + 1/(L*C)); fc =
25e3; %select bandwidth pm = 60; %select phase margin
kfb = 1; %Gain in feedback voltage measurement
Gpwm = 1; %gain of the modulator
[gain phase] = bode(Gps, 2*pi*fc);
phiboost = -90 + pm - phase; kboost
= tand(45 + phiboost/4);
gaincontroller = 1 / (kfb * Gpwm *
gain); fz= fc/ kboost; fp = fc*kboost;
kc = gaincontroller * 2*pi*fz/kboost;
wz = 2 * pi * fz; wp = 2*pi * fp; Gcs
= kc/s * ((1+ (s/wz))^2)/((1+
(s/wp))^2); Gol = Gps * Gcs;
bode(Gps),grid %Gps,Gol, Gc, Gcl
```

For $\sigma^{-1} = 5$, $K_P = 0.175$, $K_I = 9196$, $K_D = 6.66 \times 10^{-5}$

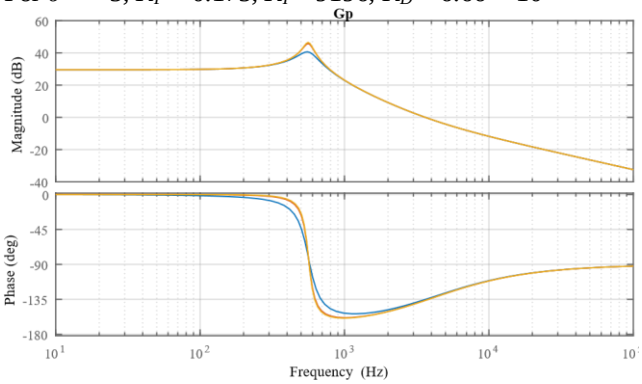

Fig. 11. Bode Plot of PID Colntrolled Buck Converter, Plant Gain

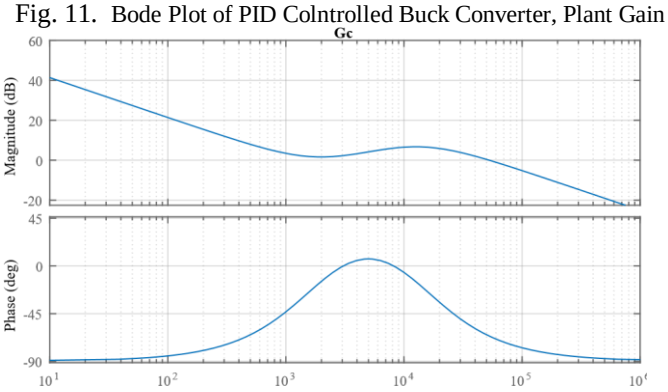

Fig. 12. Bode Plot of PID Colntrolled Buck Converter, Controller Gain

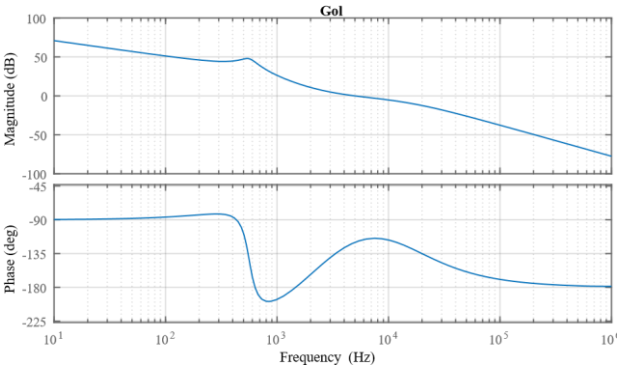

Fig. 13. Bode Plot of PID Colntrolled Buck Converter, Open-Loop Gain

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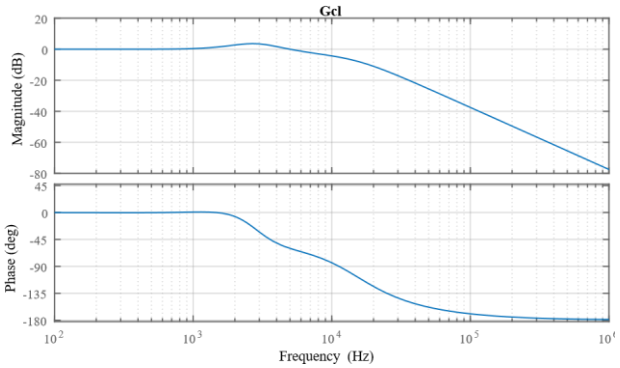

Fig. 14. Bode Plot of PID Colntrolled Buck Converter, Close-Loop Gain

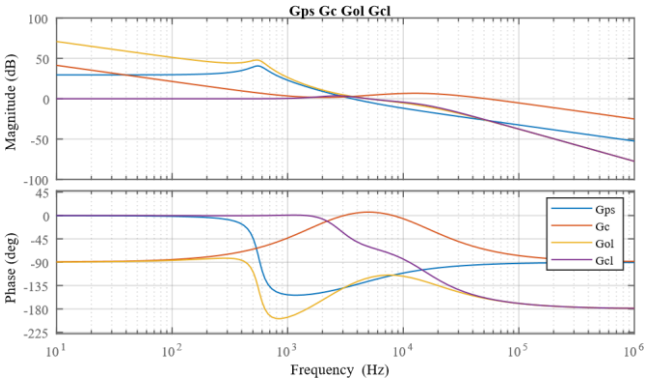

Fig. 15. Bode Plot of PID Colntrolled Buck Converter

The digital PID controller functionality in DSP is defined more by a flow chart as seen in the Fig. 16

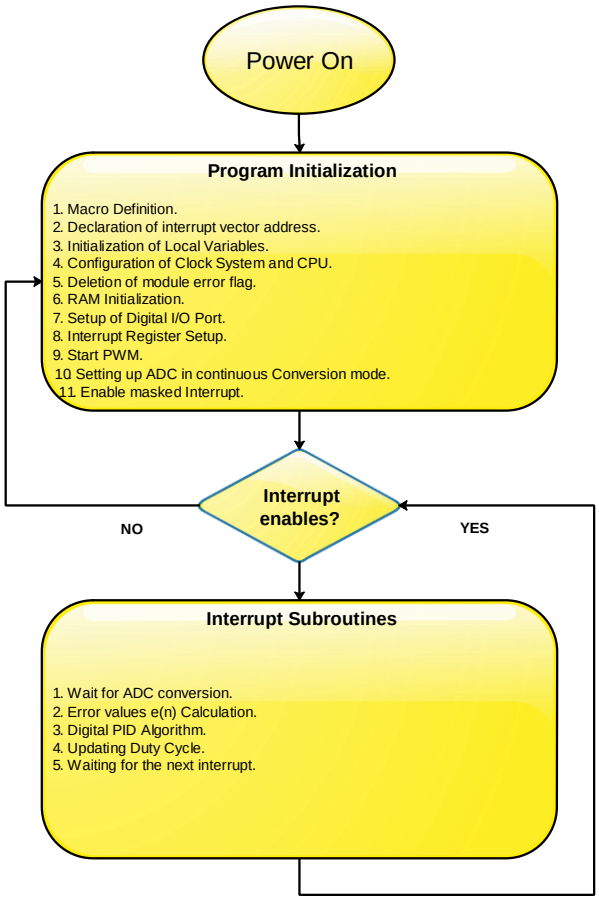

Fig. 16. Flowchart of implemented PID controller core algorithm on DSP Programs.

Aarchitecture of the digital controller is affected by sampling schemes and hence it requires proper care. For digital high power employing devices, PWM units as well as ADC are most significant device drivers within the DSP. ADC having high performance as well as PWM generators with elevated efficiency is offered by dsPIC32FJ64GS606 which allows the high specifications for the DC-DC converters to be satisfied. The ADC for dsPIC32FJ64GS606 can be activated with the help of external Pins, Event timer *EVA/B* which mainly controls and interrupts logic: underflow, timer compare, and period interrupts or with software's. In this design, ADC is activated using T2CMPR of the EVA. It generates a time base for GP Timer 2, Compare. Event Timer A, the frequency of which is expected for being equivalent to ADC's sampling frequency, as ADC's SOC i.e. Start of Conversion is programmed to cause the underflow of the timer ramp signal. This helps somewhere within the PWM cycle to change the ADC trigger point in contrast to the use of Timer 2 cycle for activating the ADC, which will correct the ADC trigger just at completion of Timer 2 period to align with the moment at which PWM had been off. This same

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SOC is initiated with the help of T2CMPR, and also the interrupt EOC i.e. End of Conversion is not activated until the conversion has been completed. After which, the interrupt routine of ADC is summoned in program. The user program reads the value transferred from the result register of ADC within the interrupt service routine ISR, introduces the developed controller and then applies the updated value for duty ratio of PWM to a relevant PWM reference register. After that, in relation to the updated duty cycle, PWM modulated value is determined and then afterwards registers are modified prior to a next ADC conversion signal. Displayed in Fig. 17 that used a Texas Instruments dsPIC32FJ64GS606 digital signal processor, DSP analysis system, is now the flowchart of an interrupt service routine to execute the control algorithm. Setting up one of it's on chip timers, adjusts the frequency of its PWM output. To control the PWM output at appropriate switching frequency, which would be 25 kHz for this research, GP Timer 1, T1 has been used. Comparison registers that are being used for writing the computed duty ratio levels are correlated with these timers. In order to obtain the PWM output, this parameter is then compared with counter value of timer. Linked PWM control registers monitor the period under which a rewritten reference value changes the original duty ratio of PWM output. These PWM control registers is defined for this research in such a way that the new value that is written in the reference register adjusts the original duty ratio of PWM output in beginning of the following timer T1 cycle.

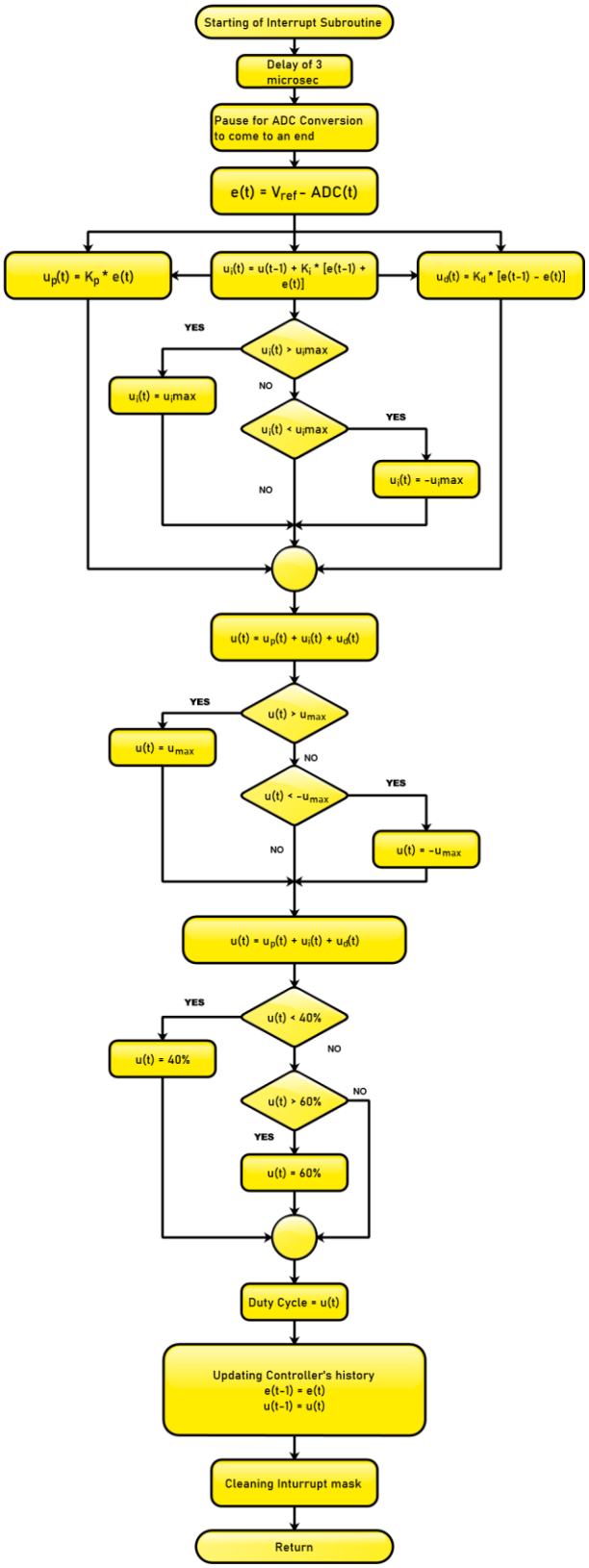

Fig. 17. Flowchart of Interrupt Service Routine.

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VI. CIRCUIT IMPLEMENTATION AND ITS OPERATION

A typical PID controller implementation of a buck converter is described in this section, with a step by step modelling procedure for practical application. Fig. 18 shows the circuit topology for the digital control of a DC-DC buck converter implementing a DSP.

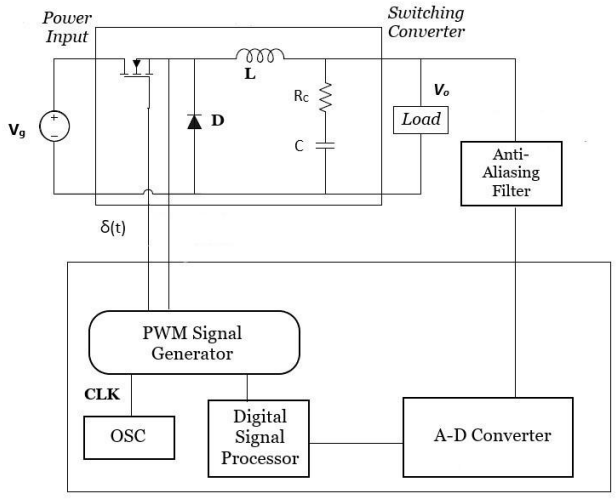

Fig. 18. Digitally operated block diagram for the buck regulator employing DSP.

According to the figure, Vg is the input voltage; V is the output voltage; R is the load resistance; I_o is the load current; D is the diode; L is the inductor used for energy storage; T_r is the switch; and C is the capacitor used for decreasing the ripple in the output. The output voltage V is transformed into a digital quantity N_n after being sent to the ADC via the antialiasing filter. This ADC's input/output relationship considers the width of quantization to be minimal and is roughly defined by the following equation without using a discrete representation:

$$N_n = G_{AD} e_n \tag{28}$$

Where the N_n, the digital quantity is a positive integer and n denotes the nth switching period. The ratio of the input and output parameters of the ADC w.r.t. output voltage is denoted by G_{ad} and its equation is

$$G_{AD} = \frac{N_{n,\max}}{V_{AD\max}} \tag{29}$$

This frequency of sampling is 100kHz and is dependent on the frequency of switching of the DC-DC buck converter. The ADC contains 8 bits from 0 to 20 V for the input region. This digital quantity N_n is then delivered to the digital signal processor (DSP). Calculation for the numerical value $N_{Ton,n+1}$ which corresponds to the ON period $Ton,n+1$ is done in the DSP. In this paper, a PID controller has been used to compute the $N_{Ton,n+1}$. Its equation is as given below:

$$N_{Ton,n+1} = N_B - K_P(N_n - N_R) - K_D(N_n - N_{n-1}) - K_I \sum (N_n - N_{INT}) \tag{30}$$

Where K_P, K_I, K_D are the proportional gain, integral gain and the derivative gain, respectively. N_B is used to denote the bias; the reference values for the proportional and integral controllers is denoted by N_R and N_{INT}, respectively:

$$N_B = N_{Ts}(1 + \frac{r}{R})\frac{V^*}{V_g} \tag{31}$$

$$N_R = N_{INT} = G_{AD} V^* \tag{32}$$

Where N_{ts} is the number corresponding to the switching period Ts. The output voltage target value is denoted by the symbol V and the internal loss resistance of the DCDC converter is denoted by r. If during the switching period f_{CK} (clock frequency) is input and a digital counter or comparator generates a PWM (pulse width modulated) signal, the representation of N_{Ts} is:

$$N_{Ts} = f_{CK} T_S \tag{33}$$

The relationship between $Ton,n+1$ and $NTon,n+1$ becomes,

$$\frac{T_{on,n+1}}{T_S} = \frac{N_{Ton,n+1}}{f_{CK} T_S} \tag{34}$$

As seen from the (34), the driving switch Tr drives the output voltage and the ON period signal T_{on} is PWM generated output with period of switching T_s.

VII. SIMULATION RESULTS

The MATLAB/Simulink ® software has been used in order to verify the PID controller in the preceding segment. This software is being used for simulating the circuit's steady-state as well as its transient characteristics. To correlate with experimental observations later, this same results obtained will be used. Fig. 19 displays the Digitally Controlled Closed-Loop Buck Converter employing a PID controller. Parasitic

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elements are used in the converter and these parameters are the calculated values

Table 2
Buck Converter Design Parameters.

Parameters	Values
Input Voltage, V_g	458V
Output Voltage, V	200V
Switching Frequency, F_s	25KHz
Inductance, L	$1.5021mH$
Capacitance, C	$0.1875\mu F$
Output Current, I_o	16A
Resistance, R	12Ω
Ripple Voltage, ΔV_C	6V
Ripple Current, Δi_L	3A

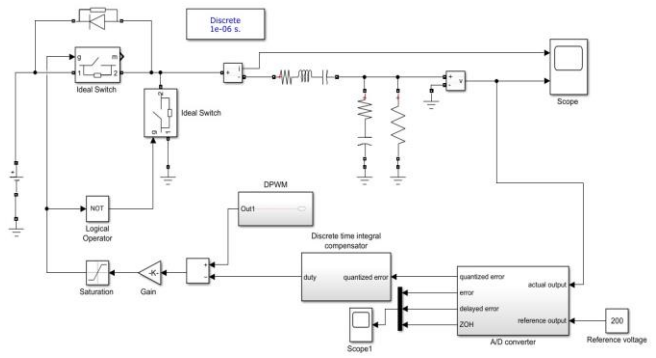

Fig. 19. MATLAB model of a Digitally Controlled Closed-Loop Buck Converter.

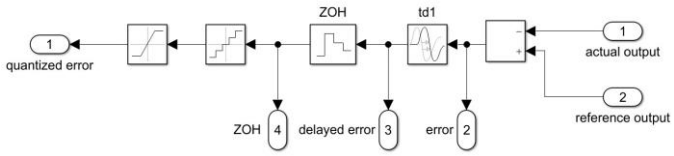

Fig. 20. Subsystem of Analog to digital Converter.

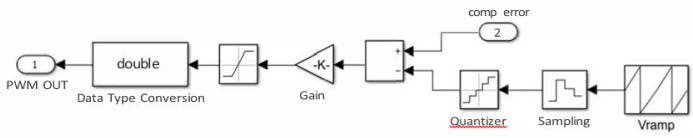

Fig. 21. Subsystem of Digital Pulse Width Modulation.

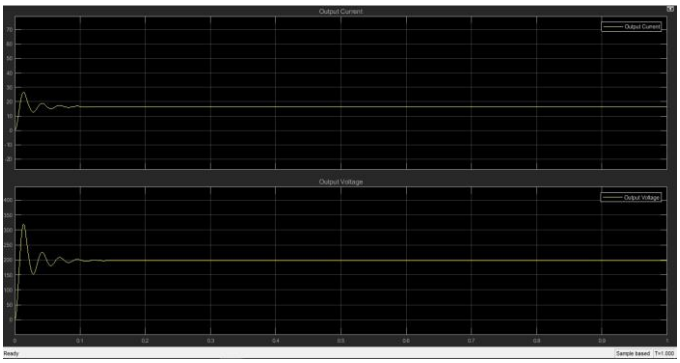

Fig. 22. Output Current and Output Voltage Waveform.

We could outline the following inference from the simulation model based on the results and waveforms above:

1. A digital simulation system is set up and the framework is provided to test out a sophisticated control scheme and much more realistic problems.
2. The offset circuitry enhances the ADC resolution, leading to a smaller error in the steady state. In fact, the amplitude of the limit cycles is improved by decreasing the resolution.
3. The effects of the simulation are not influenced mostly by delay in one switching period, but due to sampling delay, the reduced sampling frequency response dilutes the transient response.
4. When a Digital PWM resolution is lower than ADC, the limit cycle happens.

This same limit cycles are caused by quantization effects and contribute to greater steady-state error as well.

VIII. EXPERIMENTAL RESULTS

Main Function of a DC-DC converter is to convert unregulated DC voltage to a regulated DC voltage. Modern digital DC converters does have a few advantages over basic analog control. Better tolerance to technological advances, improved adaptability by modifying the programme, more efficient control methods, power control function incorporation and decreased number of components are included in the desirable circumstances. A production board from Microchip is being used for test findings. And for digital controller the 30F family dsPic controller is used here.

The aim behind this experiments would be to illustrate that digital control technology is much simpler when using a simulator with many of the functionality included. The control algorithm coefficient could be found and without possibility that perhaps the system will become unstable and then prone to oscillations. In high-power converter these Oscillations can

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be crippling. A Digitally controlled PID controller is examined experimentally.

This section summarizes the system performance of the PID controller in a DC/DC Buck converter provided to use the Procedure listed in section precedence. In this research study various parameters were varied to scrutinize the output performance of the controller. Table 3 records the output voltage of that same converter for different Voltages of input varying between 450 to 458 V. In the right hand column, the percent of the variance of its output voltage from its reference voltage is seen. It is clear from the experiment that variation on its input supply, converter has a very little impact in steady state behavior. The model's conduct during the transient start-up phase is examined in order to determine the transient behavior of the Converter. The begin transient performance of the buck Converter is examined. The settling time is roughly 0.1 ms and very little overshooting.

8.1. Performance in Steady-state

Fig. 23 shows the output current and voltage waveforms of the presented converter operating at 458V Dc supply and load of 12 ohms. From the analysis of simulation seen in Fig. 24 it is evidenced that the converter employing PID controller generates appropriate output current and voltage.

The theoretical principles are very much in line with these observations. To evaluate performance of this controller in steady-state, the supply voltage is varied from 440-458 V to see how it is feasible to retain the optimal output voltage of 200V. Fig. 25 indicates its steady-state waveforms produced underneath the normal load operation for an input voltage of 458V. Channel 1 displays the output voltage, whereas the duty cycle is given in Channel 2. Proof is provided the controller adapts new value of the duty cycle as the input voltage varies resulting in a new duty cycle which has a steady-state error of zero.

For the three separate input voltages, Table 3 indicates the converter output voltage (examined). The variance as well as the percent of its output voltage variation and the current are also seen. From the reference voltage of 200V, the deviation in output voltage is determined.

Table 3
Variation in Output Voltage employing a Digitally Controlled PID Controller.

Input Voltage	Output Voltage	Deviation(*V*)	Deviation(%)
458	199.997	-0.003	0.025
455	199.999	-0.001	0.008
453	200.002	+0.002	0.017
452	200.004	+0.004	0.034
450	199.995	-0.005	0.042

8.2. Transient response of a PID controlled Buck Converter.

The transient behaviour observation is carried out in order to evaluate the model 's stability as well as its speed response. In order to determine its transient response, that model 's activity is evaluated at the time of transient start up. From its experimental findings, it can be seen that with very few overshoot, the settling period is around 0.1s.

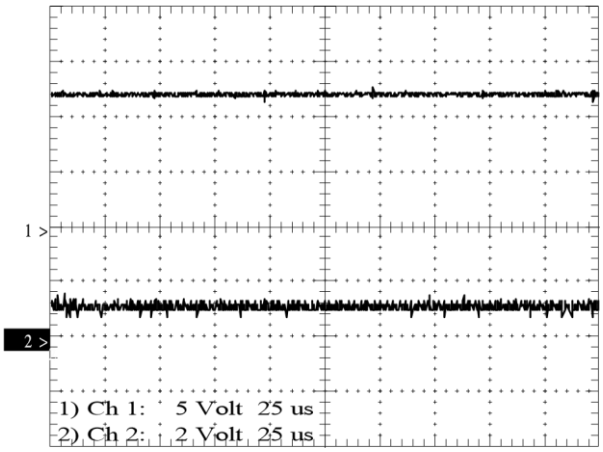

Fig. 23. Response of Buck Converter in Steady-State.

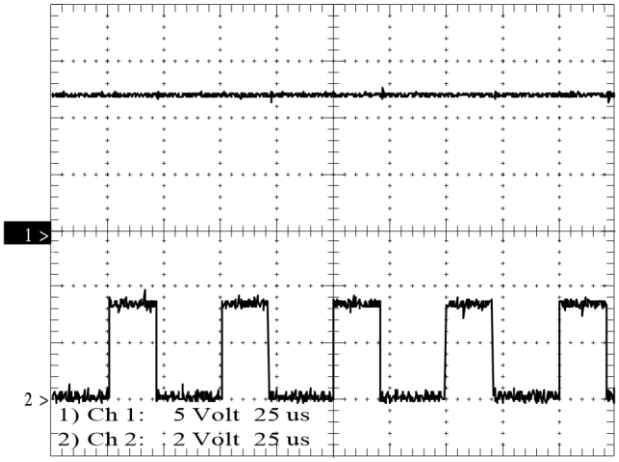

Fig. 24. New Duty Cycle of the Buck Converter.

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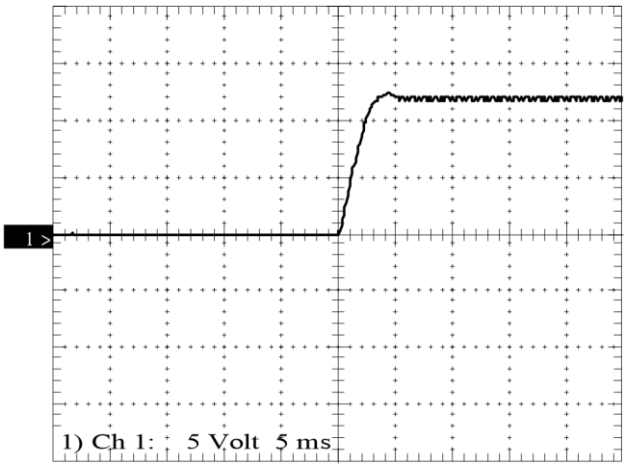

Fig. 25. Transient Response during the starting period of Buck Converter.

IX. CONCLUSION

This paper proposes the designing and implementation of digitally controlled close-loop DC-DC buck converter. A comprehensive study is provided for the design theory of a dc - dc buck converter employing a PID controller. The design considers the operational aspects of its converter into account. From the first section of this paper it can be concluded that closed loop control has less output voltage ripple than open loop operation of a buck converter. Furthermore, the results show that satisfactory steady-state characteristics can be attained while sustaining a quality transient response. About the Digital application of a controller employing DSP, design instructions are given with a simple step by step method. MATLAB/Simulink has been used for the application of a typical Buck converter with a PID controller and to model different blocks of a digital controller. To check the converter configuration and process, the experimental outcomes are provided. This experimental output is compliant with those expected simulation results of steady-state precision as well as settling time. The study suggests that one can model a switch mode power supply(SMPS) in company with good performance by using standard mathematical process along with advanced control techniques.

Declaration of competing interest / Conflict of interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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