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COMPARISON AND ANALYSIS OF PERFORMANCE PARAMETERS OF BASIC ADDERS WITH SPARSE ADDER

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***Abstract*—Adders play a vital role in the design of a digital system using VLSI (Very Large Scale Integration) technique. Adders are the basic building block of ALU (Arithmetic Logic Unit) which is an important component of a processor. In this paper we are comparing and analyzing the performance parameters of basic adders like Ripple Carry Adder, Carry Select Adder, Carry Look Ahead Adder, Parallel Prefix Adder along with sparse adder. The above mentioned adders are implemented using 90nm technology in Xilinx ISE 14.7 Suite.**

Keywords*—Ripple Carry Adder, Carry Select Adder, Carry Look Ahead Adder, Parallel Prefix Adder, Xilinx ISE 14.7 Suite.

I. INTRODUCTION

Addition is the most important operation of any digital circuit. Adders not only perform addition but also performs some basic arithmetic operations like subtraction, multiplication, increment and decrement. Adders form the heart of the digital circuit that improves the performance of the ALU which in turn increases the efficiency of the processor.

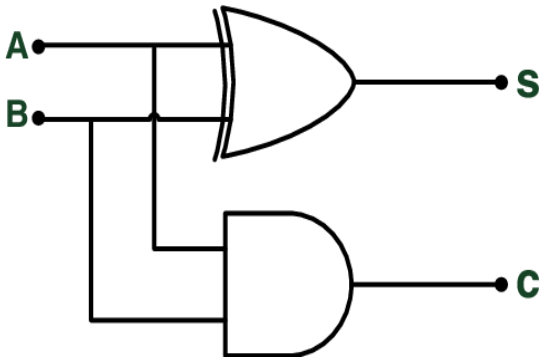
II. TYPES OF ADDERS

A. HALF ADDER

Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (S) and carry bit (C) as the output. If A and B are the input bits, then sum bit (S) is the X-OR of A and B and the carry bit (C) will be the AND of A and B. Thus Half adder circuit is constructed using one X-OR gate and one AND gate. The half adder can add only two input bits (A and B) and has nothing to do with the carry if there is any in the input.

Input		Output	
A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Truth Table of Half Adder



Circuit diagram of Half adder

B. FULL ADDER

Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM.

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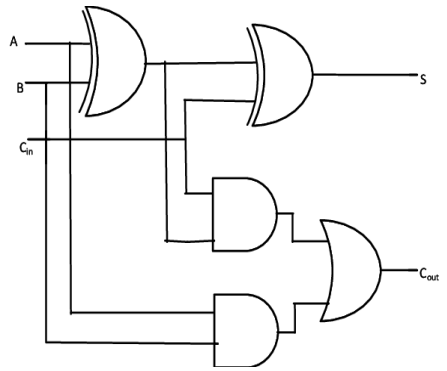
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

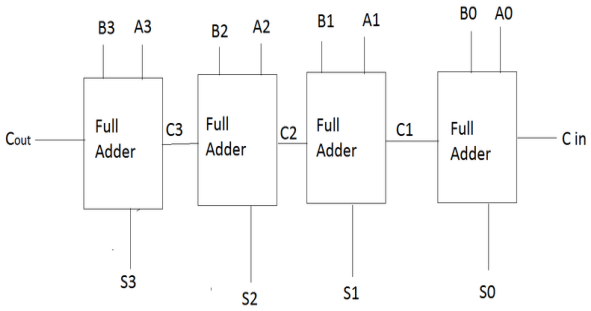
Truth table of Full adder



Circuit diagram of Full adder

C. RIPPLE CARRY ADDER

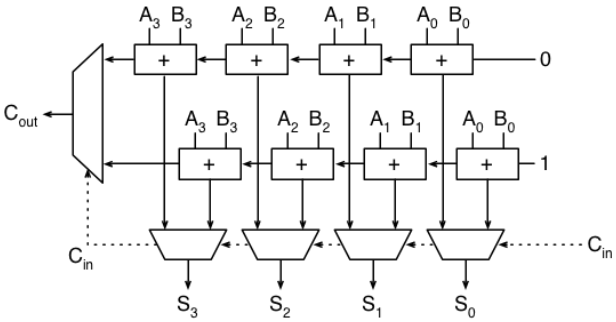
The Ripple carry adder is constructed by cascading full adder blocks in series. Each full adder is responsible for adding two binary digits at any stage. The carry-out of one stage is directly fed as the carry-in to the next stage. Each stage has to wait for the carry generated from the previous stage for computation.



Block diagram of a 4-bit Ripple carry adder

D.CARRY SELECT ADDER

The Carry select adder pre-computes the sum and carry-out for two possible cases of input carry that is when C-in = 0 and C-in = 1. The calculated sum is given to the multiplexer, which chooses the correct output depending upon the input carry coming from previous stage. This pre-computation of Sum reduces the delay of rippling of carry which is limited to only one multiplexer for each stage.



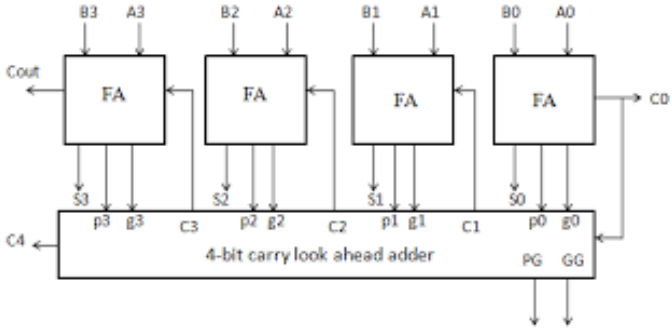
Block diagram of 4-bit Carry select adder

E. CARRY LOOK AHEAD ADDER

Carry look-ahead adder is designed to overcome the latency introduced by the rippling effect of the carry bits. This adder is based on the principle of looking at the lower order bits of the augends and addend if a higher order carry is generated. In this adder the outputs Sum and Carry are derived from the intermediate terms defined as Generate (G) and Propagate (P) terms.

Generate term: G = A.B

Propagate term: P = A⊕B.



Block diagram of 4-bit Carry Look Ahead adder

F. PARALLEL PREFIX ADDER

The Parallel prefix adder consists of three stages: pre-computation stage, prefix network stage and post-computation stage. The pre-computation stage computes the carry 'Propagate' and carry 'Generate' bits for each input pair. The prefix network stage computes the final carries from the carry 'Propagate' and carry 'Generate' bits. The final post computation stage computes the final Sum from carry generated in prefix network stage.

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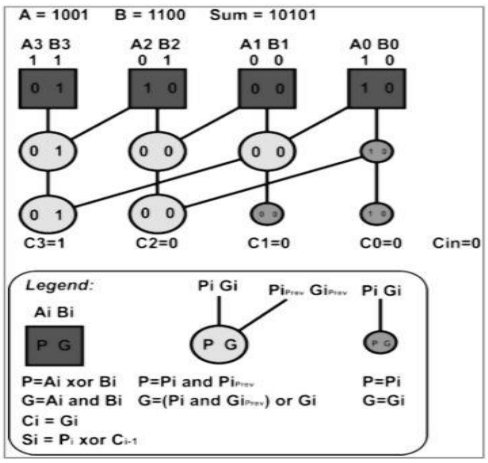


Parallel prefix adder for 4-bit

G.SPARSE ADDER

Sparse adders are highly efficient adders and are majorly known for their high speed computations. In this paper we have constructed the sparse adder as a combination of Kogge-Stone adder which is a form of parallel prefix adder along with Carry Look Ahead adder.

III. COMPARISON ANALYSIS

Comparing the basic adders like Ripple Carry Adder, Carry Select Adder and Carry Look Ahead Adder with the performance parameters: delay, power, number of bonded IOBs, number of occupied slices, total number of 4 input LUTs.

Table 1: Comparison of basic adders with performance parameters

ADDER	DELAY (ns)	POWER (mW)	NO: OF BONDED IOBs	NO: OF OCCUPIED SLICES	TOTAL NO: OF 4 INPUT LUTs
RIPPLE CARRY ADDER	12.008	68	14	6	8
CARRY SELECT ADDER	10.739	76	14	6	9
CARRY LOOK AHEAD ADDER	11.625	62	14	7	11

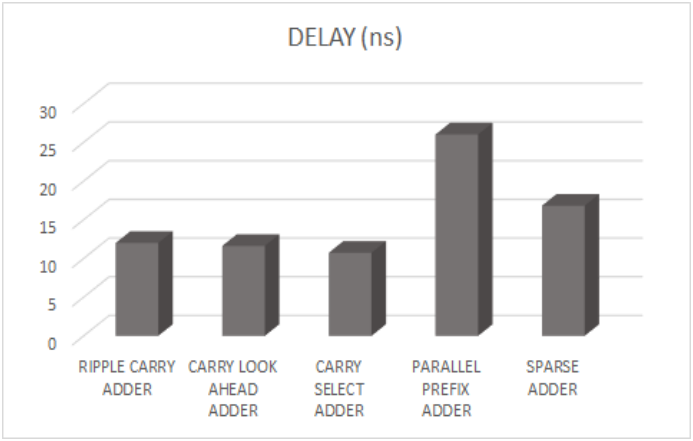
Comparing the parallel prefix adder and sparse adder with the performance parameters: delay, power, number of bonded IOBs, number of occupied slices, total number of 4 input LUTs.

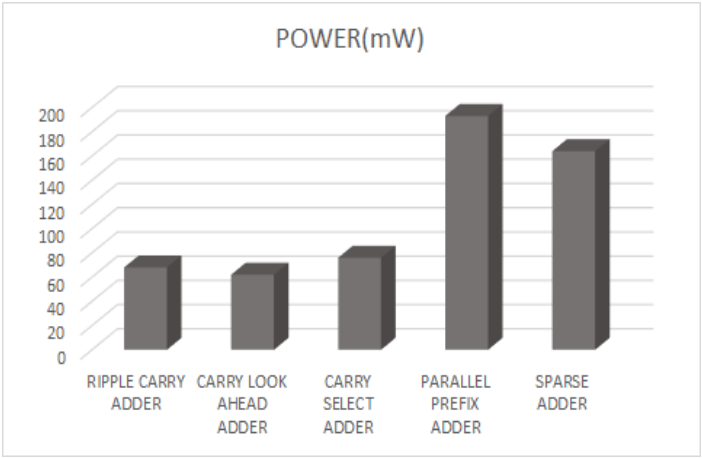
Table 2: Comparing parallel prefix adder and sparse adder with performance parameters

ADDER	DELAY (ns)	POWER (mW)	NO: OF BONDED IOBs	NO: OF OCCUPIED SLICES	TOTAL NO: OF 4 INPUT LUTs
PARALLEL PREFIX ADDER	26.012	193	49	22	42
SPARSE ADDER	16.816	164	49	39	73

IV. RESULT

In this paper sparse adder is implemented and analysed. According to the observations made sparse adder is efficient in terms of delay and power, also wiring complexity of the sparse adder is greatly reduced when compared with parallel prefix adder.





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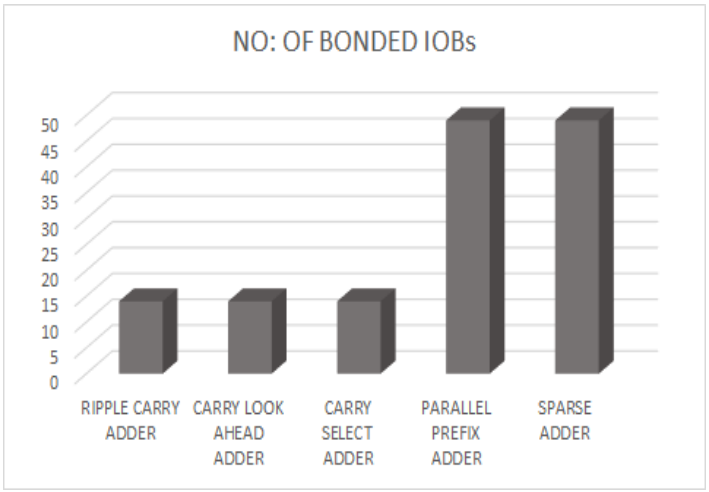
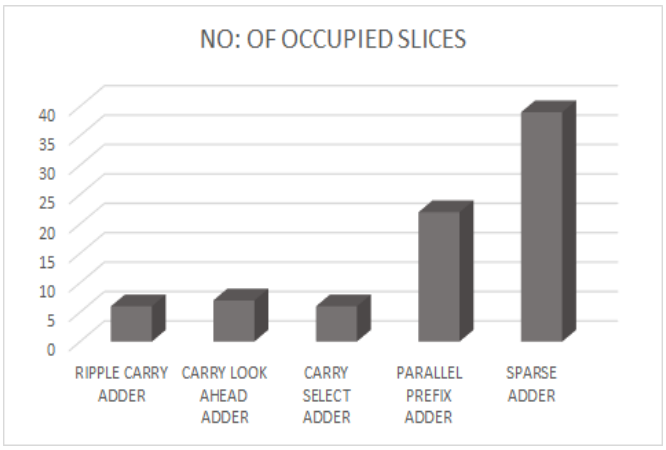
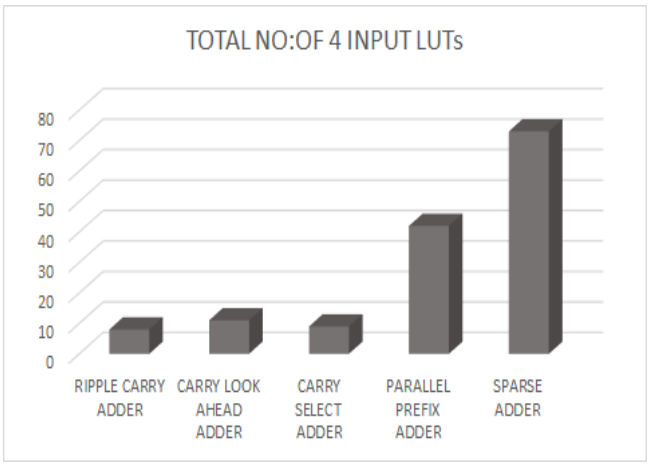
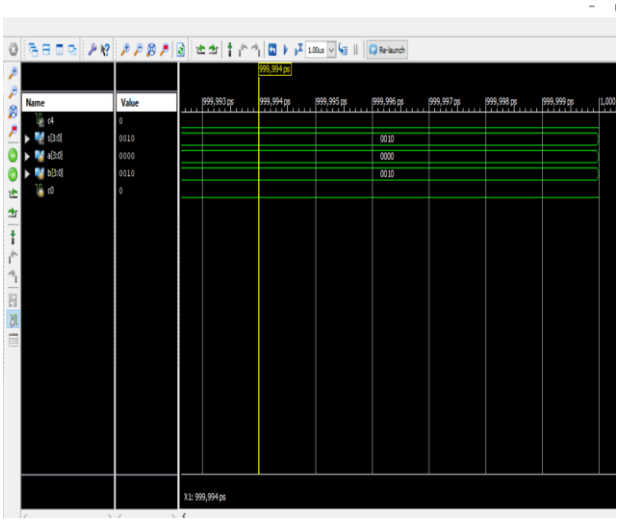


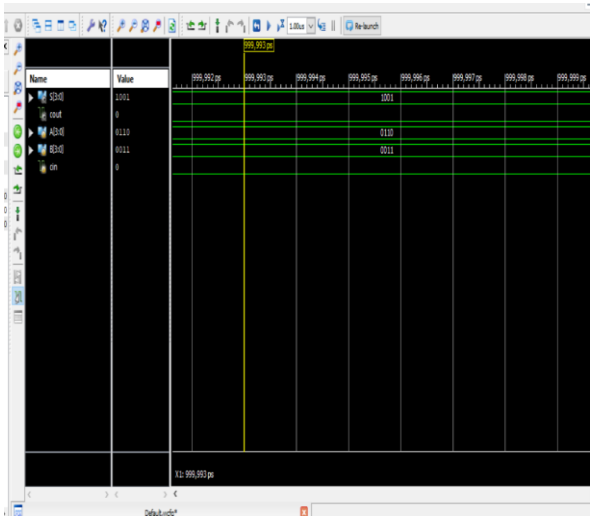




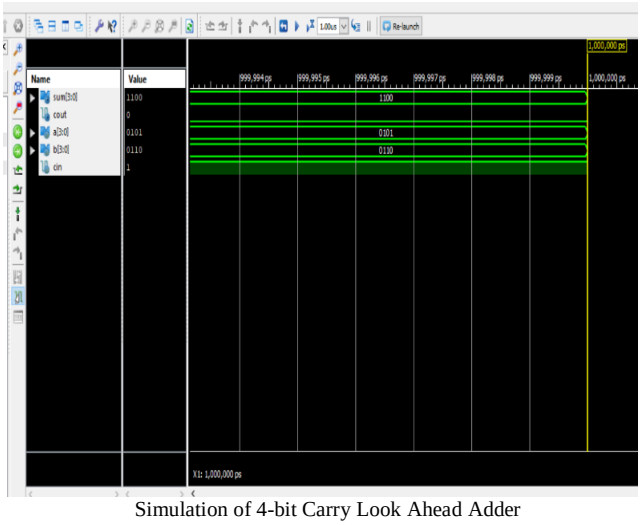
V. SIMULATIONS



Simulation of 4-bit Ripple Carry Adder



Simulation of 4-bit Carry Select Adder



Simulation of 4-bit Carry Look Ahead Adder

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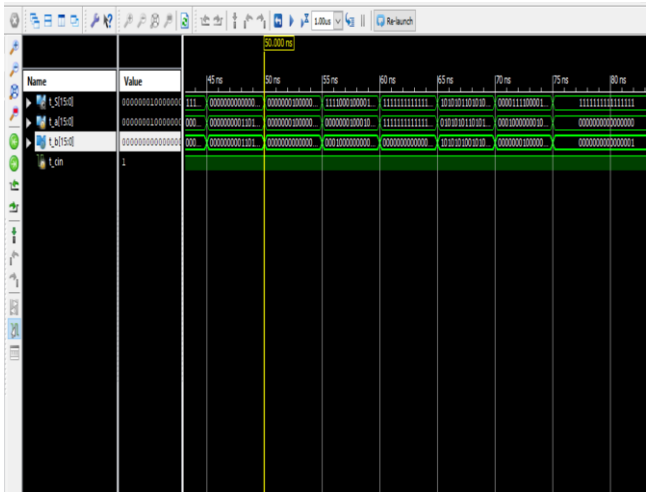
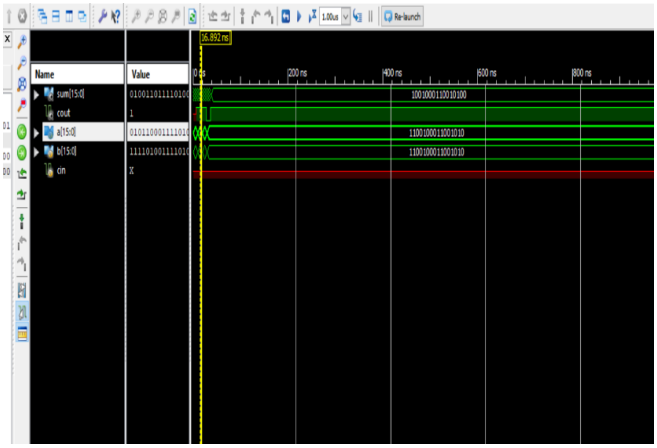


Simulation of 16-bit Parallel Prefix Adder



Simulation of 16-bit Sparse Adder

VI. CONCLUSION

In this paper we have implemented Ripple Carry Adder, Carry Select Adder, Carry Look Ahead Adder, Parallel Prefix Adder and Sparse Adder using 90nm technology in Xilinx ISE 14.7 Suite. From the comparison analysis we can conclude that sparse adder is efficient in terms of both power and delay. The delay is less for sparse adder when compared to parallel prefix adder. Power is more for carry select adder and less for sparse adder. Since sparse adder occupies more area, it can be optimized or reduced by exploring certain algorithms.

VII. ACKNOWLEDGMENT

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VIII. REFERENCES

[1] M. Sarkar, G. S. Taki, Prerna, R. Sengupta and S. N. Ray, "Design of ripple carry adder using CMOS output wired logic based majority gate," 2017 8th Annual Industrial Automation and Electromechanical Engineering Conference (IEMECON), Bangkok, 2017, pp. 328-331, doi: 10.1109/IEMECON.2017.8079617.

[2] M. Sarkar, R. Sengupta, A. Basu, D. Das, P. Saswari and P. Bhattacharjee, "Carry look ahead adder design using CMOS output wired logic based majority gate," 2017 4th International Conference on Opto-Electronics and Applied Optics (Optronix), Kolkata, 2017, pp. 1-5, doi: 10.1109/OPTRONIX.2017.8350002.

[3] J. Miao and S. Li, "A novel implementation of 4-bit carry look-ahead adder," 2017 International Conference on Electron Devices and Solid-State Circuits (EDSSC), Hsinchu, 2017, pp. 1-2, doi: 10.1109/EDSSC.2017.8126457.

[4] Junhyung Um and Taewhan Kim, "Utilization of carry-save-adders in arithmetic optimization," Twelfth Annual IEEE International ASIC/SOC Conference (Cat. No.99TH8454), Washington, DC, USA, 1999, pp. 173-177, doi: 10.1109/ASIC.1999.806498.

[5] O. J. Bedrij, "Carry-Select Adder," in IRE Transactions on Electronic Computers, vol. EC-11, no. 3, pp. 340-346, June 1962, doi: 10.1109/IRETELC.1962.5407919.

[6] Baliga, Akansha, and Deepa Yagain. "Design of high speed adders using CMOS and transmission gates in submicron technology: A comparative study." In 2011 Fourth International Conference on Emerging Trends in Engineering & Technology, pp. 284-289. IEEE, 2011.

[7] S. Parmar and K. P. Singh, "Design of high speed hybrid carry select adder," 2013 3rd IEEE International Advance Computing Conference (IACC), Ghaziabad, 2013, pp. 1656-1663

[8] Katreepalli, Raghava, and Themistoklis Haniotakis. "High speed power efficient carry select adder design." In 2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 32-37. IEEE, 2017.

[9] Saini, Jasmine, Somya Agarwal, and Aditi Kansal. "Performance, analysis and comparison of digital adders." In 2015 International Conference on Advances in Computer Engineering and Applications, pp. 80-83. IEEE, 2015.

[10] Gurjar, Prashant, Rashmi Solanki, Pooja Kansliwal, and Mahendra Vucha. "VLSI implementation of adders for high speed ALU." In 2011 Annual IEEE India Conference, pp. 1-6. IEEE, 2011.

[11] Daphni, S., and KS Vijula Grace. "A review analysis of parallel prefix adders for better performance in VLSI applications." In 2017 IEEE International Conference on Circuits and Systems (ICCS), pp. 103-106. IEEE, 2017.

[12] Yezerla, Sudheer Kumar, and B. Rajendra Naik. "Design and Estimation of delay, power and area for

Parallel prefix adders." In 2014 Recent Advances in Engineering and Computational Sciences (RAECS), pp. 1-6. IEEE, 2014.

[13] Talsania, Megha, and Eugene John. "A comparative analysis of parallel prefix adders." In Proceedings of the International Conference on Computer Design (CDES), p. 1. The Steering Committee of The World Congress in Computer Science, Computer Engineering and Applied Computing (WorldComp), 2013.

[14] Kowsalya, P., M. Malathi, and Palaniappan Ramanathan. "Low power parallel prefix adder." In Applied Mechanics and Materials, vol. 573, pp. 194-200. Trans Tech Publications Ltd, 2014.

[15] San, Aung Myo, and Alexey N. Yakunin. "Reducing the hardware complexity of a parallel prefix adder." In 2018 IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (EIConRus), pp. 1348-1351. IEEE, 2018.

[16] P. Gaharwar and A. Johari, "Design and implementation of multipliers," 2016 IEEE Students' Conference on Electrical, Electronics and Computer Science (SCEECS), Bhopal, 2016, pp. 1-4.

[17] K. N. Singh and H. Tarunkumar, "A review on various multipliers designs in VLSI," 2015 Annual IEEE India Conference (INDICON), New Delhi, 2015, pp. 1-4.

[18] M. R. Ghonge and R. S. Keote, "VLSI design of fixed width 2's compliment multiplier," 2017 International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS), Coimbatore, 2017, pp. 1-5.

[19] S. Chinthanai Selvi, R. Vigneshwari and G. Maryamirthasagayee, "Performance analysis of multiplier using various techniques," 2015 International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS), Coimbatore, 2015, pp. 1-7.

[20] B. Lamba and A. Sharma, "A review paper on different multipliers based on their different performance parameters," 2018 2nd International Conference on Inventive Systems and Control (ICISC), Coimbatore, 2018, pp. 324-327.