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IMPLEMENTATION OF VIRTUAL CHANNEL ROUTER WITH VA AND SA ARBITRATION UNIT USING VHDL

Minakshi M. Wanjari
Electronics and Telecommunication Engineering Dept.,
G. H. Raisoni College of Engineering, Nagpur, India.

Pankaj Agrawal
Electronics and Communication Engg. Dept.,
CMR Technical Campus, Hyderabad, India.

Ravi V. Kshirsagar
Electronics Engineering Dept.,
PCE, Nagpur, India.

***Abstract*—NoCs are considered the most practicable solution for many-core chips of the future. Router is the backbone of NoC which performs the essential task of guiding and coordinating the data flow and determines the performance to a large extend. This paper focuses on the implementation of virtual channel router which is considered as promising router architecture for NoC. The router consist of static virtual channel buffer architecture, router control logic and crossbar switch. Router control logic consists of virtual channel arbitration unit and switch allocation unit. The source code is written in VHDL. The router is synthesized and simulated using Xilinx ISE Design Suite 13.1. The parameters like area, frequency and delay are calculated from synthesis result. Power is calculated using Xpower analyzer. Average latency and throughput is calculated using Xilinx system generator.**

Keywords—**System on Chip(SoC); Network-on-Chip (NoC); Virtual channel (VC); Virtual channel arbitration (VA); Switch allocation (SA).**

I. INTRODUCTION

Generally, the interconnection architecture consists of dedicated wires or shared buses. If a system has a restricted number of cores then this dedicated wire architecture is efficient. With the increase in system complexity, the number of wires around the core also increases. Therefore, these dedicated wires have poor reusability and flexibility. A shared bus is a set of wires which is common to many cores. The approach of shared bus is more flexible and is totally reusable, but it permits only one communication transaction at a time, all cores share the same communication bandwidth in the system and its scalability is restricted to few dozen IP cores. Thus scalability is a major problem with buses. It is the issues in interconnection that coated the way for new paradigm in communication called the Network-on-chip (NoC)[1,2,3,4].

NoC architecture has been suggested as a high performance, scalable and power efficient alternative to the bus based architecture. It clears the scalability issue by supporting multiple concurrent connections with various systems. As system becomes more composite, more and more integration is possible to the existing system with ease without any constraints. It can minimize the wire routing congestion to a great extent. The systems that are inter connected with a network on chip can be easily replaced with other systems with any IP cores of any vendor available in the market [5].

In NoC, Router is a fundamental component which sends packets from a source to a destination router through several intermediate nodes. If the head of the packet is chocked during data transmission, the router cannot transfer the packet. In order to remove the blocking problem, the researcher advised wormhole routing method. The wormhole router splits the packet into number of flits. Buffer allocation and flit control done at a flit level in wormhole routing. Since in wormhole routing the available buffer is not allocated to the whole packet, therefore, the wormhole routing is a method which can reduces the overall latency and may decrease buffer size compared to others.

In addition to this, throughput can be increased by virtual channels which are used to avoid deadlock problem. Virtual channels dissociate the allocation of buffer space which in turn allow a flit to use a single physical channel competing with other flits. Performance of Network-on-chip depends on the router architecture to a large extend and virtual-channel router is called as the promising choice for NoC [6].

The remaining paper is prepared as section II contains the Network-on-Chip architecture; section III contains virtual channel router architecture; section IV is about the implementation and results of the design and the last section is conclusion.

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II. NoC Architecture

The Fig. 1 shows the general architecture of NoC. IP cores, routers, network interface (NI) and links are the main components of a NoC architecture [7]. IP cores are computing elements of the system such as processors, memory elements and dedicated hardware like audio and video cores, wireless transceivers etc.

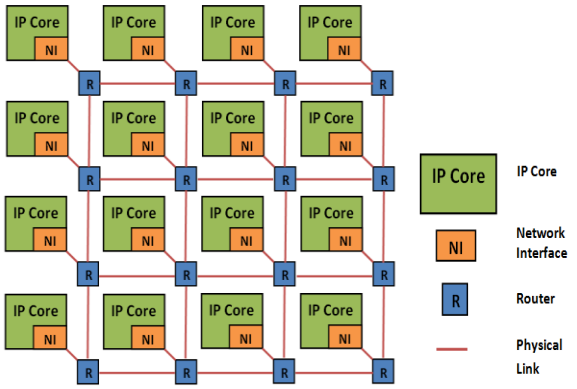

Fig. 1. NoC architecture

Router is a "much smarter buffer". It routes information from a source to destination port. It basically receives the packets from the shared links and according to the address communicated in each packet, it sends the packet to the core attached to it or to another shared link. The network interface separates the two parts computation and communication. Also acts as an inter-mediator between the router and the processing element, since each processing element has a distinct interface protocol with respect to the network. A link connects routers in the network according to the chosen topology and sets up the communication. Link is a set of wires and connects routers in the network. The concept of flits is determined at this level. A packet is split into smaller data units known as flits. Link pipelining increases the link throughput and dissociates the communication system's cycle time from the link length [8].

The network topology defines the interconnection of nodes in a network (IP cores) using links (channels). It refers to the shape of the network and how routers connect and communicate with each other. Various topologies are available like mesh, torus, tree, butterfly, polygon, and star topology [9]. But the mesh topology is preferred because of its good electrical properties, layout efficiency and simplicity in addressing resources [10]. A mesh-shaped network comprises of *m* columns and *n* rows. The routers are located in the intersections of the two wires and the IP cores are near routers. Addresses of routers and processing elements can be easily defined as *x-y* coordinates in mesh.

III. NoC Router Architecture

Router is the most important component in NoC and is called as the communication backbone of NoC. Router is used to carry out network on chip communication and it should be designed with maximum efficiency. A router is a device which can forward a data packet across the network. Routers are intelligent devices that receive incoming data packets, scrutinize their destination and work out the best path for the data to move from source to destination. Fig. 2 shows NoC router in mesh topology.

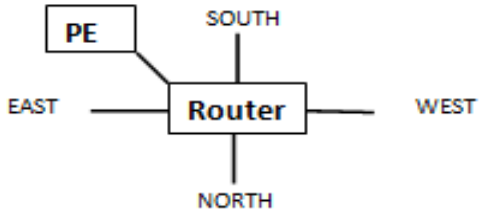

Fig. 2. NoC Router in mesh topology.

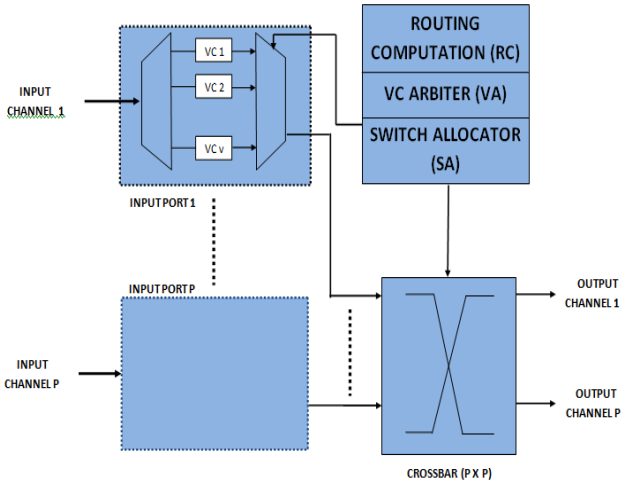

Fig. 3. Virtual Channel Router Architecture.

Generally, a NoC router has five input and five output ports. Out of which four ports are for the four directions: North, South, West, and East and fifth one is for local processing element (PE). Fig. 3 shows a virtual channel router.

This NoC router consists of three major blocks:

- Static virtual channel buffer architecture
- Router Control Logic
- Crossbar Switch

A. Static virtual channel Buffer Architecture

In virtual channel buffer architecture a physical channel is divided into a number of logic channels and these logic channels are called as virtual channels. At each input port the virtual channels (VCs) are de-multiplexed and buffered

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in FIFOs. The status information for each FIFO is kept. The FIFOs are multiplexed again on a single channel which goes to a crossbar. Virtual channel shares the bandwidth of the physical channel in a time multiplexed fashion. Virtual channels offer flexibility, better channel usage, improve network throughput and reduce the effect of blocking. Here each input port consist of 'v' virtual channels, and each virtual channel has a dedicated k-flit FIFO buffer (a flit is the smallest unit of flow control and one network packet is composed of a number of flits)[11].

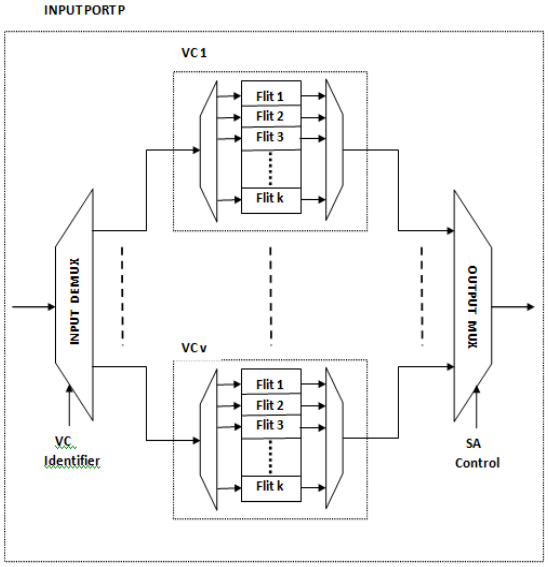

Fig. 4. Static Virtual Channel Bufer Architecture

B. Router Control Logic

The router control logic is the heart of the NoC router, and comprises of three components:

- Routing Computation (RC) unit,
- Virtual Channel Arbitration (VA) unit,
- Switch Allocation (SA) unit, and

1) *Routing Computation (RC) unit :* The RC unit is used for directing the header flit of an incoming packet to the appropriate output Physical Channel (PC) and/or dictating valid output Virtual Channels (VC) within the selected PC. RC is a "per-packet" operation; it is performed once for each packet within a router.

2) Virtual Channel Arbitration (VA) Unit : The Virtual Channel Arbitration (VA) unit arbitrates amongst all packets requesting access to the same VCs and decides on winners. Two arbitration stages are generally required.

a) *VA1:* Reduces the number of requests from each input VC to one; and this ensures the request of a single VC at a particular output port by each input VC. A total of Pv v:1 arbiters are required in the first arbitration stage (see Fig. 5.) one arbiter for each input VC.

b) *VA2*: The winning request from first arbitration stage proceeds to the second arbitration stage. A total of Pv Pv:1 arbiters are required in this stage. One arbiter is required for each output Virtual Channel.

VA is also a "per-packet" operation; it is only performed on header flits.

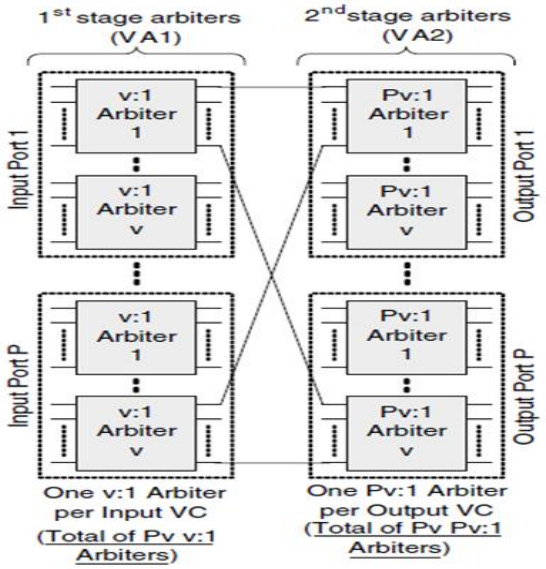

Fig. 5. Virtual Channel Arbitration (VA) Unit

3) *Switch Allocation (SA) Unit:* The Switch Allocation unit arbitrates between all VCs requesting access to the crossbar and grants permission to the winning flits. Switch allocation also has two stages.

a) *SA1:* Accounts for the sharing of a single port by a number of VCs. All VCs in the same input port compete with each other locally for access to the output physical channels. Number of arbiters required for SA1 are P v:1 (i.e. one arbiter per input port).

b) *SA2:* Arbitrates between the winning requests from each input port competing for each output port. The SA2 stage sets the crossbar control signals accordingly. Number of arbiters required for SA2 are P P:1(i.e. one arbiter per output port) as shown in fig. 6.

SA is a "per-flit" operation, i.e. it is performed on all flits passing through the router, not just header flits. The SA winners are then able to cross the crossbar and are directed towards the respective output links.

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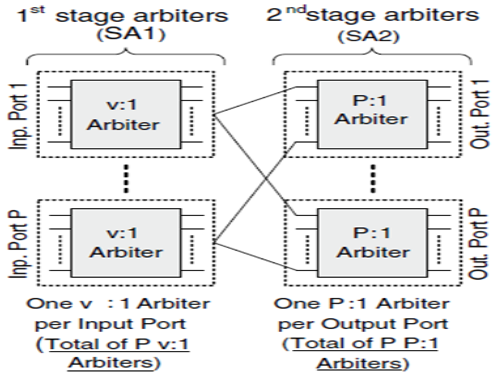

Fig. 6. Switch Allocation (SA) Unit.

C. Crossbar Switch

The crossbar switch in the design is used for physically connecting an input port to its destined output port. Flits that have been allowed to pass on the crossbar are passed to the appropriate output channel. In the architecture shown in Figure 3, each input port is forced to share a single crossbar port even when multiple flits could be sent from various virtual channel buffers. This limitation allows the crossbar size to be kept small and independent of the number of virtual channels [12]. Dally [13] and Chien [14] suggest that providing a single crossbar input for each physical input port will have small impact on performance as the data rate out of each input port is limited by its input bandwidth.

IV. Implementation And Results

The router design is implemented in VHDL on structural Register Transfer Level (RTL). It is synthesized and simulated in Xilinx ISE Design Suite 13.1. The router is prototyped in Spartan3 xc3s400. Simulation refers to the verification of a design, its function and performance. It is the process of applying stimuli to a model over time and producing corresponding responses from a model. A test bench is also written to test the routing pattern for various data packets. The reset (rst) signal must be kept low during normal operations. The data1, data2, data3, data4, data5 are input signals given to the router. The routing pattern is observed from the output signals dout1, dout2, dout3, dout4, dout5. The data at the input ports is directed to the output port depending on the first three bits of the input data which act as the select lines of the de-multiplexer. The simulation result for NoC router is shown in fig. 7. Table I shows the synthesis results of the NoC router which shows the area required by the router. The operating frequency of this router is 74.368MHz as shown in fig. 8. Minimum input arrival time before clock is 3.898ns and maximum output required time after clock is estimated as 6.280ns. The minimum clock period required is 13.447ns. The power is calculated using Xpower analyzer. The static power is 0.060W, dynamic power is 0.017W and total power is 0.077W as shown in fig. 9. The latency and throughput is calculated by using Xilinx System Generator, the average-latency is 39 clocks(fig. 10) and throughput percentage is 20.008(fig. 11).

TABLE I. Synthesis Result Showing Area of NoC Router.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	2232	3584	62%
Number of Slice Flip Flops	2962	7168	41%
Number of 4 input LUTs	2164	7168	30%
Number of bonded IOBs	82	221	37%
Number of GCLKs	1	8	12%

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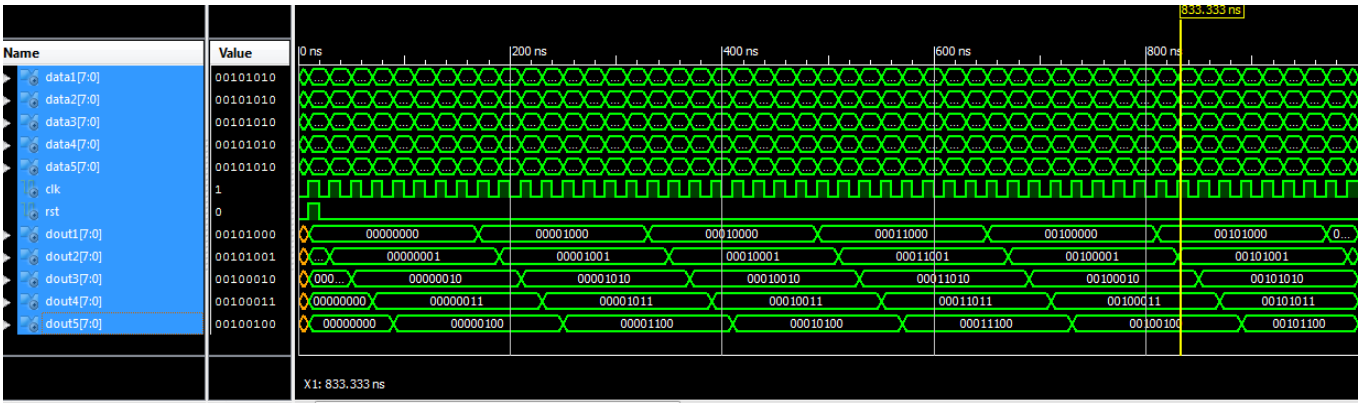

Fig. 7. NoC Router Simulation.(simulation of VCA & SA)

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Minimum period: 13.447ns (Maximum Frequency: 74.368MHz)
Minimum input arrival time before clock: 3.898ns
Maximum output required time after clock: 6.280ns
Maximum combinational path delay: No path found
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Fig. 8. Frequency and Delay

Device	
Family	Spartan3
Part	xc3s400
Package	fg320
Grade	Commercial
Process	Typical
Speed Grade	-5

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

Characterization	
PRODUCTION	v1.2,06-25-09

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.007	1	---	---
Logic	0.002	2169	7168	30
Signals	0.007	4336	---	---
IOs	0.001	82	221	37
Leakage	0.060			
Total	0.077			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	24.1	83.2	26.8

Supply Summary Source	Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.200	0.030	0.014	0.015
Vccaux	2.500	0.015	0.000	0.015
Vcco25	2.500	0.002	0.000	0.002

Supply Power (W)	Total	Dynamic	Quiescent
	0.077	0.017	0.060

Fig. 9. Power Analysis showing dynamic, static and total power.

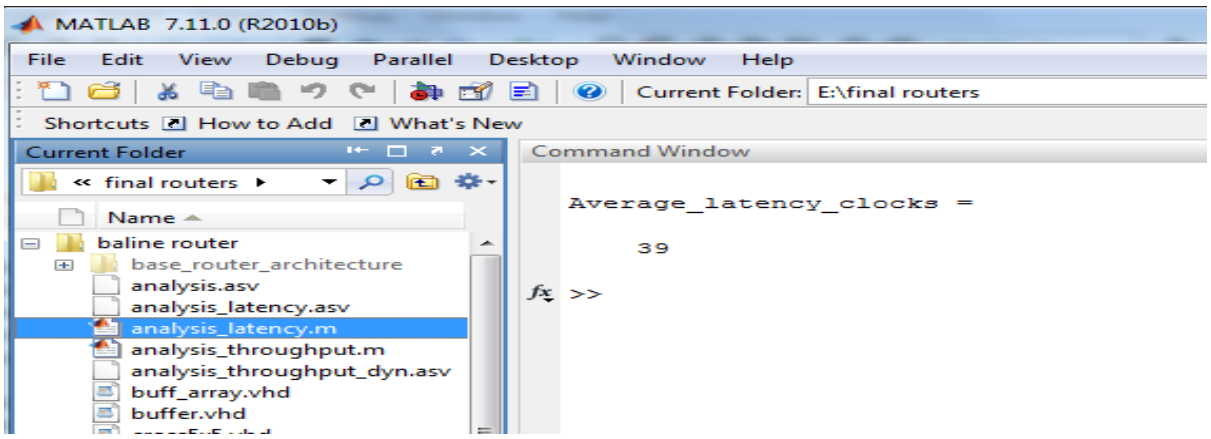

Fig. 10. Average Latency.

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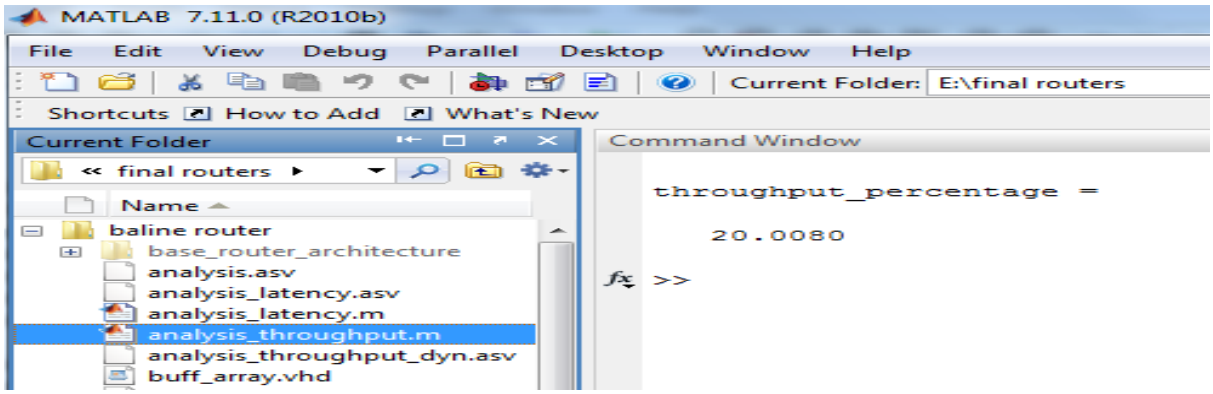

Fig. 11. Throughput Percentage.

V. CONCLUSION

A five port virtual channel NoC router with virtual channel arbitration unit and switch allocation unit is proposed in this paper and in order to analyze the area, frequency, delay and power consumption it is implemented in RTL VHDL. In this router the virtual channels minimizes the head of blocking problem. As virtual channels are fixed in numbers for each input port so it is used for network traffic other than heavy network traffic. The virtual channel arbitration and switch allocation arbitration units use round robin arbiters which are used for fair arbitration. The RTL synthesis and the simulation of the router is done in Xilinx ISE design suite 13.1 tool. The functionality of NoC router is shown by the simulation result. This router is used in NoCs where less power, less area with reduced HoL blocking is the requirement. This work can be modified for better channel utilization, less latency and high throughput to make it more efficient as the NoC performance depends on the design of the router architecture.

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