International Journal of Engineering Applied Sciences and Technology, 2020
Vol. 4, Issue 11, ISSN No. 2455-2143, Pages 191-198
Published Online March 2020 in IJEAST (http://www.ijeast.com)

LEAKAGE POWER CONSUMPTION IN DOMINO CIRCUITS FOR WIDE-FAN-INPUTS USING HIGH THRESHOLD STACKED TRANSISTORS

Vinothkumar K
Assistant Professor,
Department of ECE,
N.S.N College of Engineering and
Technology, Karur, Tamilnadu, India.

Venkatesh M
Research Scholar,
Thiagarajar College of Engineering, Madurai,
Tamilnadu, India.

***Abstract*---In domino logic circuits, scaling down technology threshold voltage is decreases the subthreshold and gate oxide leakage or static power dissipation can be performed. In this paper, we introduced new domino logic circuits to reduce leakage power in the circuitry. High threshold n-type and p-type transistors inserted between precharge and evaluation network, the gate of these transistors are connected and controlled by the respective drain region. For any combination of input vectors, the inserting two transistors creates stack thereby increasing the propagation delay from the path supply voltage to ground. Wide fan-in result designed by using 16nm V2.1 HP Predictive technology model CMOS Technology. In this model, the active and standby power consumption is observed at different 25^0C and 110^0C temperature variations. The maximum power consumption 91% is achieved when compared to the conventional circuits. Performance can be increased due to decreasing the output voltage swing.**

Keywords - **GALEOR, Domino logic circuits, Sub-threshold leakage, Static power dissipation, Leakage current.**

I. INTRODUCTION

Domino logic could be a CMOS-based evolution of the dynamic logic techniques that is predicated on either PMOS or NMOS transistors. It permits a rail-to-rail logic swing and is developed to increasing the circuit speed. Using this technique, glitch-free operation may be obtained as every gate will create only one transition. However the most drawbacks are that of the charge distribution. The key necessity of making use of CMOS domino logic for the look of combination logic circuits is that of low tolerance and high speed operation. Dynamic logic like domino logic is wide employed in several applications to attain high performance, that can't be achieved with static logic designs. However, the most disadvantages of dynamic logic families is that they're additional sensitive to noise than static logic families. On the opposite hand, because the technology scales down, the availability voltage is reduced for low power, and therefore the threshold voltage (Vth) is additionally scaled all the way down to come through high performance. Since reducing the threshold voltage exponentially will increase the sub-threshold leakage current, reduction of leakage current and rising noise immunity square measure of major concern in strong and superior styles in recent technology generations, particularly for wide fan-in dynamic gates. Less threshold voltage suggests that smaller gate change trip purpose in domino circuits. Smaller trip points create the domino circuit additional at risk of input noise.

A conventional approach to enhance the hardiness of domino circuits is keeper transistor upsizing. However, as the keeper transistor is upsized, the contention between keeper transistor and NMOS evaluation network will increase within the evaluation phase. Such current contention will increase evaluation delay of the circuit and will increase power dissipation. Thus, keeper upsizing trades off delay and power to enhance noise and leakage immunity. Such trade-off is not acceptable as a result of it may build the circuit too slow or too power. There are techniques proposed within the literature to address this issue. High speed domino logic and conditional keeper are among the foremost effective solutions for raising the robustness of domino logic. In this paper, we introduce a new domino circuit for wide fan-input, high speed and low power VLSI applications in ultra deep submicron technology.

The rest of this paper is arranged as follows. Section II Analysis of Leakage Reduction Technique, Section III Proposed New Domino Logic Circuits, Section IV Simulation results and

International Journal of Engineering Applied Sciences and Technology, 2020
Vol. 4, Issue 11, ISSN No. 2455-2143, Pages 191-198
Published Online March 2020 in IJEAST (http://www.ijeast.com)

discussion for the proposed circuit using T-SPICE simulations in 16-nm high-performance predictive technology compared with other conventional circuits and Section V includes conclusion.

II. ANALYSIS OF LEAKAGE REDUCTION TECHNIQUE

As the scaling down technology the threshold voltage decreases the sub threshold leakage and static power dissipation are increased in the path between supply voltages to ground. There are several techniques to reduce the leakage in CMOS circuits. Now we introduced a Galeor technique to reduce the leakage power in domino logic circuits. Galeor is a gated leakage control transistor shown in figure 1. It consists of n-type and p–type transistor connecting between the precharge and evaluation network. The gate of the inserting transistors are connected and controlled by the respective drain region. For any combination of input vectors these inserting transistor creates the stack thereby increasing the delay in the circuitry the leakage can be reduced from supply voltage to ground. The advantage of the Galeor technique is not affected the dynamic power and does not required any control logic signal and self control.

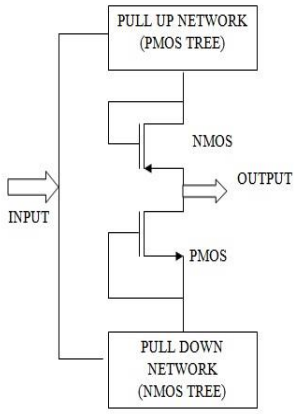


Figure.1. GALEOR Technique

In this technique reduces the output voltage swing because of the threshold voltage loss caused by the addition MOS transistors. Reduced voltage swing will increase the propagation delay through the circuit. Area is decreased by eliminating the use of control logic to modify between the active and standby states. Performance can be increased because of the reduced output voltage swing.

A) Derivation of Threshold Estimation:

Threshold voltage (V_{th}) estimation of high threshold stacked GALEOR is obtained by applying KCL at simple node of output. By which the relationship between drain to source current of n type and source to drain current of p type gate leakage control transistor (GLT) is given by

$$I_{dsn} = \left| - I_{dsp} \right| \quad (1)$$

The two transistors are in linear or in non saturation region,

$$I_{dsp} = \mu_p C_{ox} \frac{w_p}{L_p} \left[\left(V_{gsp} - V_{tp} \right) N V_{ds} - 0.5 N V_{ds}^{\,2} \right] \quad (2)$$

$$I_{dsn} = \mu_n C_{ox} \frac{w_n}{L_n} \left[\left(V_{gsn} - V_{tn} \right) N V_{ds} - 0.5 N V_{ds}^{\,2} \right] \quad (3)$$

By substituting the equation (2) and (3) in (1) and we get

$$\beta_n \left[\left(V_{gsn} - V_{tn} \right) N V_{ds} - 0.5 N V_{ds}^{\,2} \right] = \beta_p \left[\left(V_{gsp} - V_{tp} \right) N V_{ds} - 0.5 N V_{ds}^{\,2} \right] \quad (4)$$

With

$$\beta_p = \mu_p C_{ox} \frac{w_p}{L_p} \text{ And } \beta_n = \mu_n C_{ox} \frac{w_n}{L_n} \quad (5)$$

By solving the equation (4) for V_{tn}, if $V_{gsn}=V_{gsp}=V_{gs}$ we get

$$V_{tn} = \frac{\beta_p}{\beta_n} V_{tp} + \left(1 - \frac{\beta_p}{\beta_n} \right) V_{gs} - 0.5 N V_{ds} \left(1 - \frac{\beta_p}{\beta_n} \right) \quad (6)$$

If $V_{gsn} \neq V_{gsp}$

$$V_{tn} = V_{gsn} + \frac{\beta_p}{\beta_n} \left(V_{tp} - V_{gsp} \right) + 0.5 N V_{ds} \left(\frac{\beta_p}{\beta_n} - 1 \right) \quad (7)$$

By solving the equation (4) for V_{tp}, if $V_{gsn}=V_{gsp}=V_{gs}$ we get

$$V_{tp} = \frac{\beta_n}{\beta_p} V_{tn} + \left(1 - \frac{\beta_n}{\beta_p} \right) V_{gs} - 0.5 N V_{ds} \left(1 - \frac{\beta_n}{\beta_p} \right) \quad (8)$$

If $V_{gsn} \neq V_{gsp}$

$$V_{tp} = V_{gsp} + \frac{\beta_n}{\beta_p} \left(V_{tn} - V_{gsn} \right) + 0.5 N V_{ds} \left(\frac{\beta_n}{\beta_p} - 1 \right) \quad (9)$$

where V_{tp} is the threshold voltage of PGLT, V_{tn} is the threshold voltage of NGLT, V_{gs} is gate to source voltage of transistor, V_{ds} is drain to source voltage of transistor, W_n and W_p are width of NGLT and PGLT respectively,

L_p and L_n are length of PGLT and NGLT respectively, $c_{ox}=\varepsilon/t_{ox}$ is gate oxide capacitance with ε is relative permittivity and t_{ox} is the gate oxide thickness, and μ_n and μ_p are the mobility of electrons and holes respectively of the GALEOR network.

By providing different voltage at the point node V_{dd} the maximum current consumed, operating region and the resistance of GALEOR for different threshold voltage are shown in the figure 2. It is certainly proved that the GALEOR operates in

International Journal of Engineering Applied Sciences and Technology, 2020
Vol. 4, Issue 11, ISSN No. 2455-2143, Pages 191-198
Published Online March 2020 in IJEAST (http://www.ijeast.com)

linear region for different voltage and it will provide high resistance when threshold voltage is high**.**

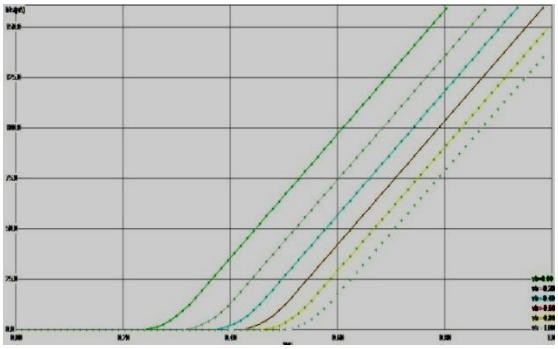


Figure.2. Output graph of GALEOR drawn by varying different node V_{dd} voltage with different threshold voltage

III. PROPOSED DOMINO LOGIC CIRCUITS

A) Dual V_{th} Standard Footerless Domino Logic Circuit:

The first standard dual Vth transistor was introduced by kao. It can be classified into footed and footerless domino. The footerless domino logic operates at idle and non-ideal modes. When pull up network (PUN) MP1 is connected to the clock signal transition is said to be precharge phase and then pull down network (PDN) MN2 is connected to the input signal transition is called as evaluation phase. The output of these phases is connected through the skewed inverter this node is known as dynamic node. The output of the inverter is connected through the keeper transistor. The feedback keeper transistor PMOS is used to avoid any undesired discharging at the dynamic nodes against noise, leakage current, charge sharing problem and hence increasing the robustness. The ratio of keeper transistor (K) is distinct as,

$$K = \frac{\mu p(W/L)keeper-transistor}{\mu n(W/L)evaluation-network} \qquad (10)$$

Although keeper transistor improves the noise immunity, it will increase current conflict between the keeper transistor and the evaluation network, thus the circuit increases power optimization and delay of standard domino circuit. Working of Dual-threshold domino logic: When the clock is low or non-ideal mode operation MP1 precharge transistor is ON and the dynamic node takes place, then the node is called as precharge phase. During the precharge output node goes to high then the MP2 transistor turns ON due to skewed inverter at the dynamic node maintaining high state. The domino logic output is independent of the input vectors applied at the evaluation network, and then outflow current is dependent on the input vectors applied. Alternatively when the clock is high or ideal mode operation MP1 transistor is OFF condition and the dynamic node depends on the input vector is applied, MP2 transistor is also depended on the output of the circuit this phase is known as evaluation network. I_{sub} and Igate also depends only the input vectors applied in the circuits.

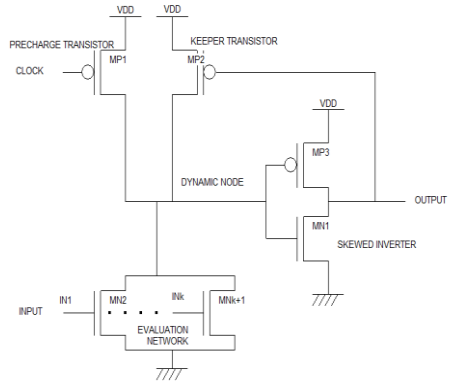


Figure.3. Standard Dual-Vth Domino Logic OR gate

B) GALEOR Standard Footerless Domino Circuit:

In this dual threshold domino logic circuit consists of three modes: precharge, evaluation and dynamic node. In this technique, we introduced an effective stacked n-type and p-type transistor connecting between the pull up network (PUN) and pull down network (PDN). The gate region of these transistors is connected through the respective drain region. For all input vector combinations inserting two transistors creates stack, thereby increasing delay in the circuitry then the sub-threshold and gate oxide leakage current or static power dissipation will be deduced simultaneously.

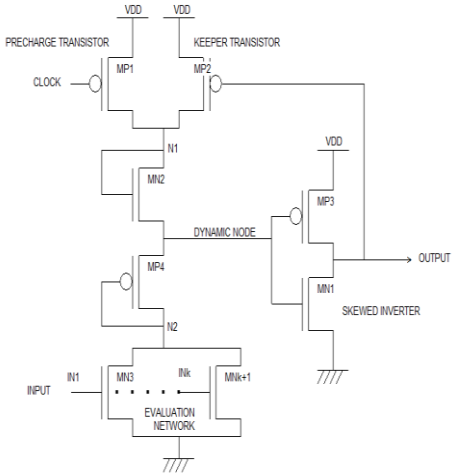


Figure.4. Proposed standard dual Vth domino logic OR gate

In our approach, MN2 (NMOS) and MP4 (PMOS) two gate leakage controlled transistors are

International Journal of Engineering Applied Sciences and Technology, 2020
Vol. 4, Issue 11, ISSN No. 2455-2143, Pages 191-198
Published Online March 2020 in IJEAST (http://www.ijeast.com)

inserted between the precharge transistor and evaluation network. The gate of these transistors are connected and controlled by the drain region respectively. In this configuration, MN2 and MP4 transistor switching operation depend on the voltage probable at N1 and N2 nodes respectively. As far as this any combination of input, inserting transistor creates stack effect, Due to increasing delay in the path between supply voltage and ground, the leakage current can be decreased.

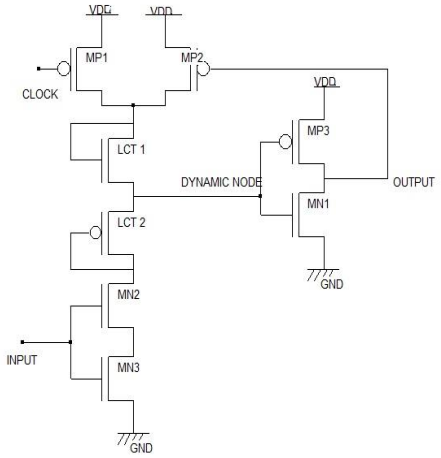


Figure.5. Proposed standard dual Vth domino logic AND gate

C) Circuit Operation:

When the clock is low or non-ideal mode MP1 transistor is ON condition and the dynamic node takes place, then the node N1 is charging then the MN2 transistor turns ON condition. Due to the dynamic node is charged high then the output of the inverter is more sufficient to turn ON the MP2 transistor. Suppose if the inputs of the evaluation network are low then the node N2 charging due to MP4 transistor is in ON condition less resistivity path then the circuit introduced delay between the supply voltage and ground or if the inputs are high then the voltage node N2 is not sufficient to turn on the MP4 transistor goes to create stack effect. Due to dynamic node maintaining the high charging, this phase is called as precharge phase. The domino logic circuit output is independent of the input vectors applied at the evaluation network, and then leakage current is dependent on the input vectors applied.

Now the clock is high or idle mode this phase is called as evaluation network. Charging and discharging of the dynamic node depends upon the input vector applied. If the inputs are less MP4 transistor is ON condition then the dynamic node gets charged by the evaluation network and the output of the skewed inverter is low, it is more sufficient to turn ON the MP2 transistor. Due to the node N1 goes to turn ON the transistor MN2, and then the transistors create stack effect, between supply voltage and ground. Thereby reducing the I_{sub}, I_{gate} leakage current and static power dissipation. A further way if all the inputs are high at the evaluation network, the dynamic knot will be discharged. The output of the inverter is high; the transistor MP2 reaches OFF condition at the node of N1 transistor MN2 and then the transistors create stack effect, between power supply and ground. It also increases the propagation delay through the path in the circuitry simultaneously, and then the delay can be controlled by sizing of the gate leakage controlled transistors.

In this paper, the proposed method is applied to the various domino logic circuits such as Conditional Keeper Domino (CKD), High Speed Domino (HSD), Leakage Current Replica Keeper Domino (LCR Keeper), and Controlled Keeper by Current Comparison Domino (CKCCD), Diode Footed Domino (DFD), Diode Partitioned Domino (DPD), and Current Comparison Domino (CCD).

IV. SIMULATION RESULT AND DISCUSSION

PTM- Predictive Technology model is used for simulating the standard dual-Vth domino logic and proposed technique circuits for accurate estimation of sub-threshold and gate oxide leakage currents. Following currents are simulated in a 16nm high performance CMOS technology, Vtp= -0.43121 and Vtn= 0.47965V, V_{DD}= 0.8V and output capacitance Cout=1pF) at different die temperature 25^0c and 110^0c respectively. The output waveforms are obtained by T-SPICE simulation using the parameters with specified values mentioned above.

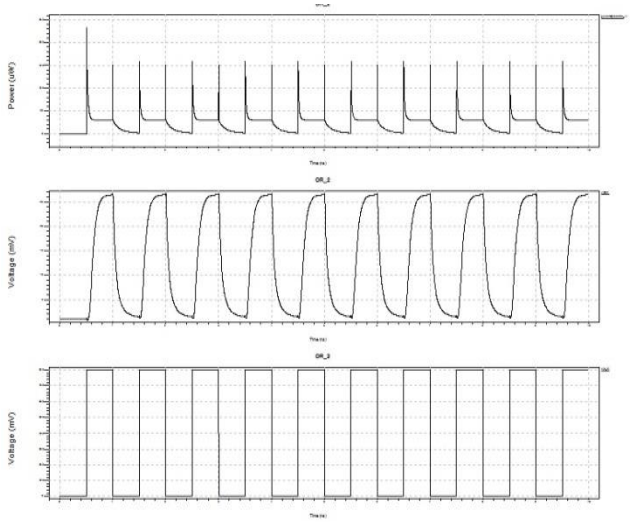


Figure.6. Instantaneous power, Output waveform and Input waveform

Leakage current consumption in domino logic is reduced by the GALEOR network. Reduction in leakage current is obtained by reducing sub threshold leakage and gate oxide leakage current or static power dissipation by stack effect, thereby increasing the delay in the circuit between supply

International Journal of Engineering Applied Sciences and Technology, 2020
Vol. 4, Issue 11, ISSN No. 2455-2143, Pages 191-198
Published Online March 2020 in IJEAST (http://www.ijeast.com)

voltage and ground node using GALEOR Thus the maximum power reduction is obtain when compared with 64 bit, 32 bit, 16 bit and 8 bit wide fan in domino logic gate with PTM V2.1 of 16nm technology at a power supply of 0.8V in SPICE simulation and results are tabulated in table 1 and 2 at different temperature variation 25^0C and 110^0C.

TABLE.1 COMPARISON OF POWER CONSUMPTION BASECASE Vs PROPOSED METHOD *($T=110^0C$)*

DOMINO Circuits		**POWER CONSUMPTION ANALYSIS (microwatts)**							
Wide-Inputs Temp=110^0C		**BASECASE**				**PROPOSED METHOD**			
		8	**16**	**32**	**64**	**8**	**16**	**32**	**64**
SFLD	**Power**	244.69	225.98	160.64	94.73	32.52	16.70	10.32	16.47
	N.power	1	1	1	1	0.49	0.05	0.02	0.01
CKCCD	**Power**	160.07	325.43	108.31	717.47	74.57	17.26	2.284	8.261
	N.power	1	1	1	1	0.46	0.05	0.02	0.01
CKD	**Power**	174.93	33.61	64.43	38.21	160.44	8.792	5.644	7.122
	N.power	1	1	1	1	0.91	0.26	0.08	0.18
DFD	**Power**	908.74	7575	7970	1563	6.850	2.453	13.99	25.30
	N.power	1	1	1	1	0.003	0.0006	0.001	0.01
DPD	**Power**	1754	1749	177.2	463.4	1173	606.07	31.46	51.61
	N.power	1	1	1	1	0.67	0.3	0.17	0.11
HSD	**Power**	176.89	160.60	243.91	245.60	142.02	125.26	30.39	51.72
	N.power	1	1	1	1	0.80	0.77	0.12	0.21
LCR	**Power**	45.52	8.966	26.23	29.02	30.76	3.664	18.98	22.66
	N.power	1	1	1	1	0.67	0.40	0.72	0.78
CCD	**Power**	188.62	418.16	309.21	93.79	93.87	24.73	8.374	1.069
	N.power	1	1	1	1	0.13	0.07	0.06	0.17
LCK	**Power**	15.70	16.23	16.53	16.67	3.325	3.353	3.348	3.378
	N.power	1	1	1	1	0.21	0.20	0.20	0.20

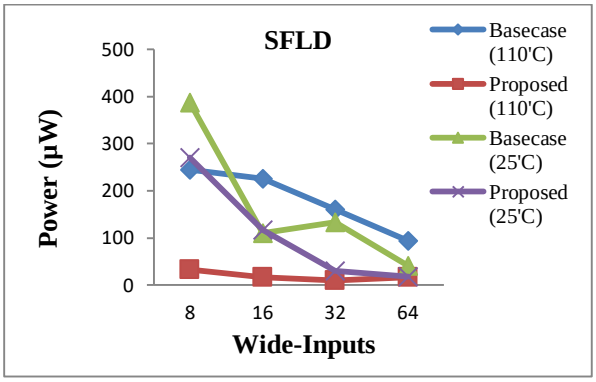
TABLE.2 COMPARISON OF POWER CONSUMPTION BASECASE Vs PROPOSED METHOD *($T=25^0C$)*

DOMINO Circuits		**POWER CONSUMPTION ANALYSIS (microwatts)**							
Wide-Inputs Temp=25^0C		**BASECASE**				**PROPOSED METHOD**			
		8	**16**	**32**	**64**	**8**	**16**	**32**	**64**
SFLD	**Power**	388.16	110.90	132.88	40.82	271.08	117.10	30.795	17.793
	N.power	1	1	1	1	0.85	0.97	0.65	0.74
CKCCD	**Power**	693.76	166.49	514.44	683.20	170.83	144.24	56.40	10.50
	N.power	1	1	1	1	0.25	0.86	0.10	0.01
CKD	**Power**	286.91	63.194	28.87	133.45	32.64	13.75	18.99	14.701
	N.power	1	1	1	1	0.11	0.21	0.65	0.11
DFD	**Power**	1189	8936	9446	2347	443.33	304.79	6.893	22.412
	N.power	1	1	1	1	0.37	0.03	0.0007	0.01
DPD	**Power**	374.3	1097.7	1052.2	673.85	353.31	729.15	828.36	106.71
	N.power	1	1	1	1	0.94	0.66	0.78	0.15
HSD	**Power**	223.58	203.19	488.38	472.71	111.78	55.83	331.06	252.50
	N.power	1	1	1	1	0.49	0.27	0.67	0.53
LCR	**Power**	35.31	16.73	11.58	13.59	2.483	9.846	2.384	2.774
	N.power	1	1	1	1	0.07	0.58	0.20	0.20
CCD	**Power**	289.99	341.51	466.48	170.83	247.76	332.68	306.41	127.20
	N.power	1	1	1	1	0.69	1.05	0.23	0.43

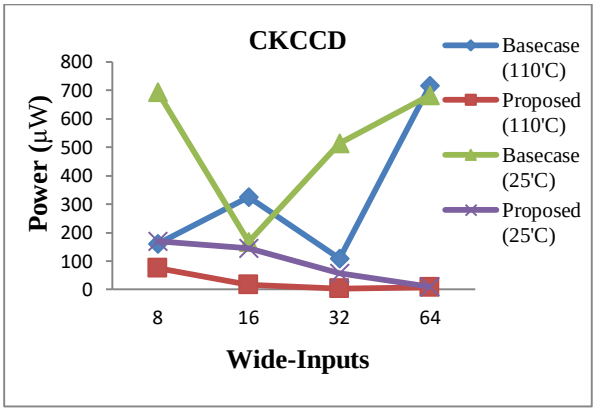
International Journal of Engineering Applied Sciences and Technology, 2020
Vol. 4, Issue 11, ISSN No. 2455-2143, Pages 191-198
Published Online March 2020 in IJEAST (http://www.ijeast.com)

LCK	**Power**	14.33	14.65	14.87	15.08	2.042	2.130	2.253	2.375
	N.power	1	1	1	1	0.14	0.14	0.15	0.15

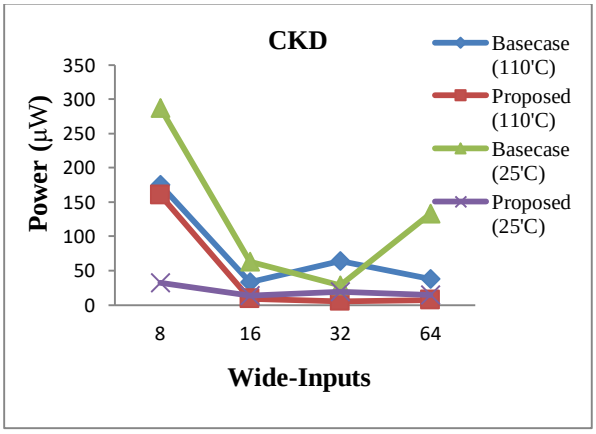
N.power= Normalized Active Power Consumption



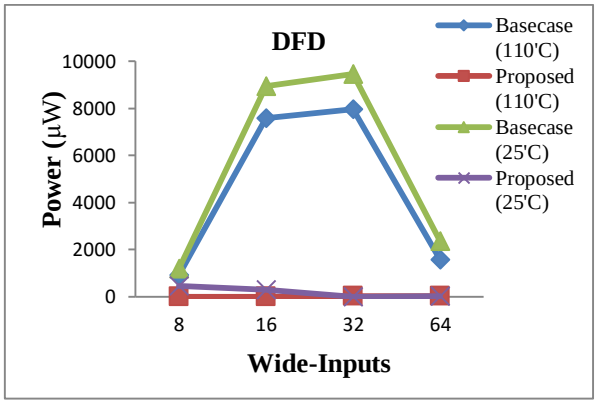
(a)



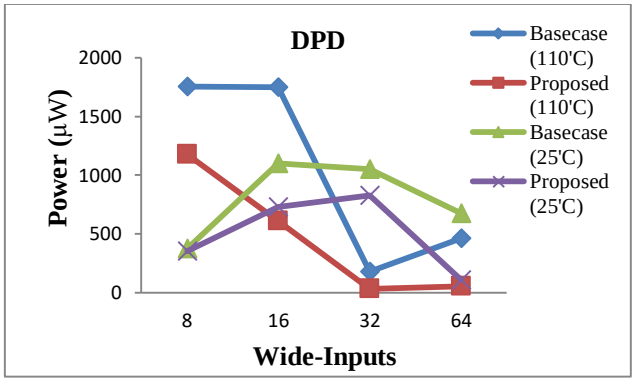
(b)



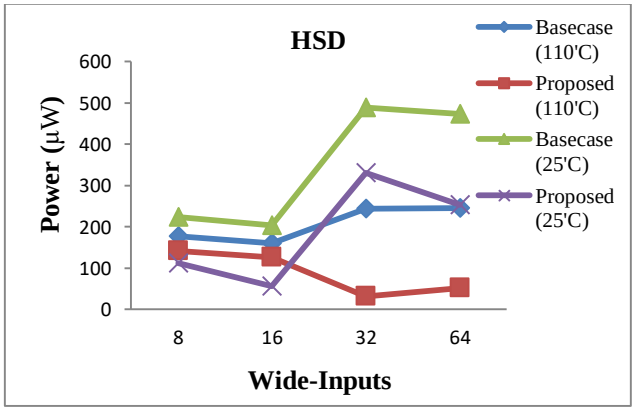
(c)



(d)

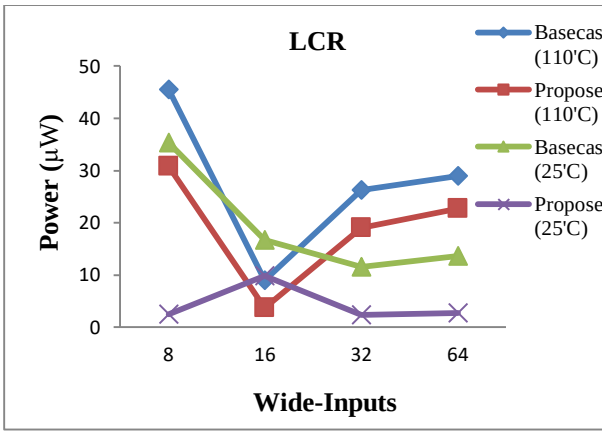


(e)

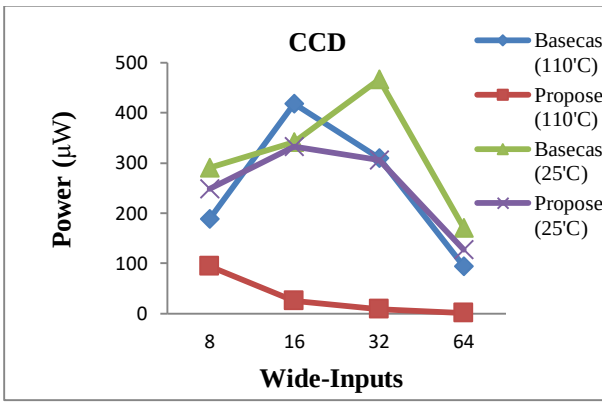


(f)

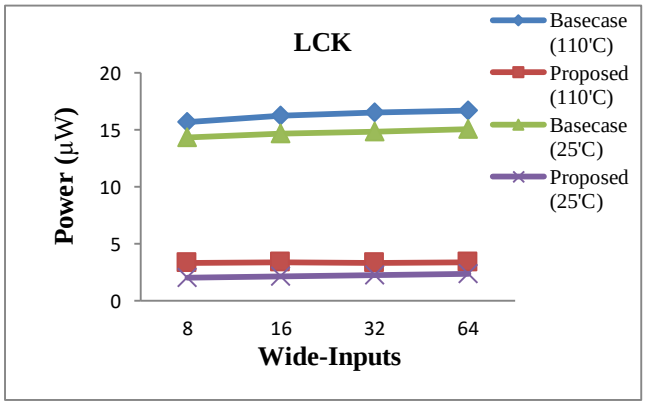
International Journal of Engineering Applied Sciences and Technology, 2020
Vol. 4, Issue 11, ISSN No. 2455-2143, Pages 191-198
Published Online March 2020 in IJEAST (http://www.ijeast.com)



(g)



(h)



(i)

Figure.7(a)(b)(c)(d)(e)(f)(g)(h)(i): Comparison result of the proposed method and the basecase maximum active power can be deduced in the various circuits at 110^0C and 25^0Cdifferent die temperature

V. CONCLUSION

In this paper, a new low-leakage and high speed domino logic circuits for low power VLSI applications using high threshold stacked transistors. Proposed circuits obtained excellent noise immunity and higher speed compared to the other dominos. These dominos not affected the dynamic power dissipation and switching power activity. The gate oxide leakage is suppressed by evaluation phase and the subthreshold leakage is suppressed by precharge phase at both 25^0C and 110^0C temperature variations. The maximum leakage power consumption obtained when compared to conventional circuits at 16nm HP PTM V2.1 CMOS Technology.

VI. REFERENCES

[1] Peiravi, A., & Asyaei, M. (2013). Current-Comparison-Based Domino: New Low-Leakage High-Speed Domino Circuit for Wide Fan-In Gates. IEEE Transactions on VLSI Systems, 21(5), Pp: 934-943. doi:10.1109/tvlsi.2012.2202408

[2] Katrue, S., & Kudithipudi, D. (2008). GALEOR: Leakage reduction for CMOS circuits. 2008 15th IEEE International Conference on Electronics, Circuits and Systems. doi:10.1109/icecs.2008.4674918

[3] Lei Wang, Krishwamurthy, R. K., Soumyanath, K., & Shanbhag, N. R. (2000). An energy-efficient leakage-tolerant dynamic circuit technique. Proceedings of 13th Annual IEEE International ASIC/SOC Conference. doi:10.1109/asic.2000.880705

[4] Mahmoodi-Meimand, H., & Roy, K. (2004). Diode-Footed Domino: A Leakage-Tolerant High Fan-in Dynamic Circuit Design Style. IEEE Transactions on Circuits and Systems I: 51(3). doi:10.1109/tcsi.2004.823665

[5] A. Alvandpour, R. Krishnamurthy, K. Sourrty, and S. Y. Borkar, (2002) "A sub-130-nm conditional-keeper technique," IEEE J. Solid-State Circuits, vol. 37, no. 5, Pp. 633–638.

[6] Anis, M. H., Allam, M. W., & Elmasry, M. I. (2002). Energy-efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies. IEEE Transactions on VLSI Systems, 10(2), Pp:71–78. doi:10.1109/92.994977.

[7] Lih, Y., Tzartzanis, N., & Walker, W. W. (2007). A Leakage Current Replica Keeper for Dynamic Circuits. IEEE Journal of Solid-State Circuits, 42(1), Pp: 48–55. doi:10.1109/jssc.2006.885051

[8] Peiravi, A., & Asyaei, M. (2012). Robust low leakage controlled keeper by current-comparison domino for wide fan-in gates. Integration, the VLSI Journal, 45(1), Pp: 22–32. doi:10.1016/j.vlsi.2011.07.002

[9] Suzuki, H., Kim, C. H., & Roy, K. (2007). Fast Tag Comparator Using Diode Partitioned Domino for 64-bit Microprocessors. IEEE Transactions on Circuits and Systems I: 54(2), Pp: 322–328. doi:10.1109/tcsi.2006.885998

[10] Bowman, K. A., Duvall, S. G., & Meindl, J. D. (2002). Impact of die-to-die and within-die

parameter fluctuations on the maximum clock frequency distribution for gigascale integration. IEEE Journal of Solid-State Circuits, 37(2), Pp: 183–190. doi:10.1109/4.982424

[11] Dadgour, H. F., & Banerjee, K. (2010). A Novel Variation-Tolerant Keeper Architecture for High-Performance Low-Power Wide Fan-In Dynamic or Gates. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 18(11), Pp; 1567–1577. doi:10.1109/tvlsi.2009.2025591

[12] Kim, C. H., Roy, K., Hsu, S., Krishnamurthy, R., & Borkar, S (2006). A process variation compensating technique with an on-die leakage current sensor for nanometer scale dynamic circuits. IEEE Transactions on VLSI Systems, 14(6), Pp:646–649. doi:10.1109/tvlsi.2006.878226

[13] Soutedeh Hamedi-Hagh, Sooseok OH, Ahmet Binchal & Dae-Hee Park, (2008) Designing of next generation Amplifiers using Nanowire FET's, Journal of Electrical Engineering and technology, Vol 3, No. 4, Pp.566-570.

[14] Mostafa, H., Anis, M., & Elmasry, M. (2011). Novel Timing Yield Improvement Circuits for High-Performance Low-Power Wide Fan-In Dynamic OR Gates. IEEE Transactions on Circuits and Systems I: Regular Papers, 58(8), Pp: 1785–1797. doi:10.1109/tcsi.2011.2107171

[15] Hanchate, N., & Ranganathan, N. (2004). LECTOR: a technique for leakage reduction in CMOS circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 12(2), Pp: 196–205. doi:10.1109/tvlsi.2003.821547