International Journal of Engineering Applied Sciences and Technology, 2022
Vol. 6, Issue 9, ISSN No. 2455-2143, Pages 272-274
Published Online January 2022 in IJEAST (http://www.ijeast.com)

CONDITIONAL DISCHARGE FLIPFLOP

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***Abstract*— In this paper, high-performance flip-flops are classified into two categories: the conditional precharge and the conditional capture technologies. This classification is mainly done to reduce the switching activities. Here a flip-flop is introduced that is the conditional discharge flipflop. It is based on the conditional discharge technology. This CDFF will reduce the switching activities and produces less glitches at the output.**

***Index Terms*—Digital CMOS, flip-flop, low power, very large scale integration (VLSI).**

I. INTRODUCTION

Many microprocessors make use of master-slave and pulse-triggered flip-flops. Master-slave flip-flops are made up of two stages, one master and one slave. These master slaves are characterized by hard edge property whereas pulse triggered flipflops are characterized by soft edge property and has a single stage. The main advantages of pulse-triggered flip-flops is that they allow time borrowing. They provide higher performance than their master-slave. Pulse-triggered flip-flops are classified into two types, implicit and explicit, and this classification is based on what pulse generator they use. In implicit-pulse triggered flip-flops, the pulse is generated inside the flip-flop, in explicit-pulse triggered flip-flops, the pulse is generated externally.

Explicit- pulse triggered flip-flops consumes more energy as the pulse is generated externally. However, Explicit- pulse triggered flip-flops has several advantages. It can have the pulse generator that can be shared by neighboring flip-flops. This sharing can help in distributing the power overhead of the pulse generator and it also increases efficiency when compared to implicit pulse triggered flipflops.

The dynamic behavior results in the wastage of power due to the internal switching activity. Reducing these activities can result in reducing the overall power dissipation. Several existing approaches to reduce the switching activity are surveyed and are classified into conditional precharge and conditional capture techniques. This paper reviews these techniques with some associated flip-flops utilizing these techniques. Also, a new technique, Conditional Discharge, is proposed in this paper. This new technique not only reduces the internal switching activity of flip-flops but also overcomes the limitations associated with some of the techniques mentioned above.

II. TECHNIQUES TO REDUCE SWITCHING ACTIVITIES

Flip-flops are generally dynamic in nature, and some internal nodes are precharged and evaluated in each cycle without producing any useful activity at the output when the input is stable. Reducing this redundant switching activity can result in reduction of power dissipation. A survey of such techniques is conducted, and the main techniques were classified into conditional precharge and conditional capture.

A. Conditional Precharge Technique

Fig. 1 shows the general idea of the conditional precharge technique. There are two phases. One is precharge phase and the other is evaluation phase.

When in precharge phase, the clk is made LOW and the control signal is switched on through which the node x is charged to vdd. When in evaluation phase clk is made LOW and x would be the complement of the input D.

B. Conditional Capture Technique

Fig .2 shows the general structure of conditional capture technique. Considering the circuit when the clk is LOW the node x is precharged to vdd. when clk turns HIGH based on the switching of the control signal node x will be the complement of the input D.

There are many disadvantages in this model.one of the main disadvantage is that it consumes more power. Hence to overcome this, a new technique is proposed that reduces the switching activity there by reducing the power dissipation.

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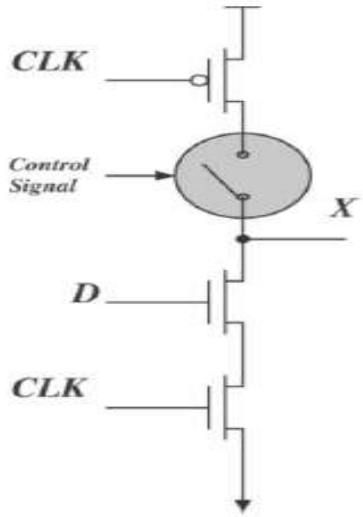

Fig 1. Conditional precharge technique

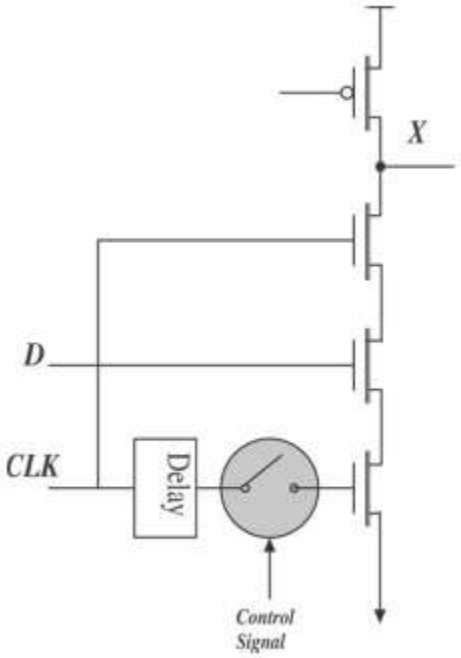

Fig. 2. Conditional capture technique

III. PROPOSED CONDITIONAL DISCHARGE TECHNIQUE

A new technique has been proposed so that we have the minimum power dissipation. As per the fig3 the extra switching activity is eliminated by controlling the discharge path when the input is stable HIGH and, thus, the name Conditional Discharge Technique. In this scheme, an nMOS transistor controlled by qb is inserted in the discharge path of the stage with the high-switching activity. When the input undergoes a LOW-to-HIGH transition, the output changes to HIGH and to LOW. Switching of the discharge path is done by the transition of output stage to prevent it from discharging or doing evaluation.

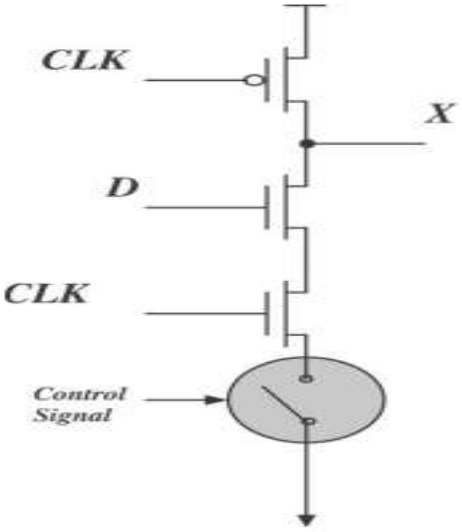

Fig. 3. Proposed conditional precharge technique

The schematic diagram of the proposed flip-flop, conditional discharge flip-flop (CDFF), is shown in Fig. 4. From the schematic, the working is as follows.
When the clk is LOW the node x is precharged to vdd and the next stage hold the previous value. When clk turns HIGH, if the previous value stored is low at qb then based on the data given, it will decide to whether sample the input at the output or hold the previous state. Node X stays HIGH or precharged in most cases, which helps in simplifying the keeper structure as shown in Fig. 4, and it also reduces the capacitive load at node X.

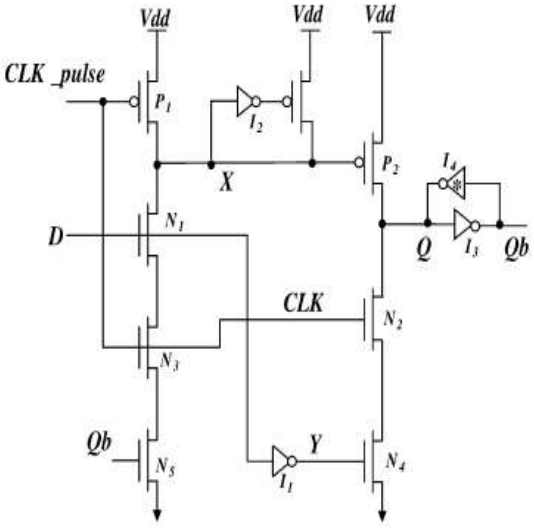

Fig. 4. Proposed conditional discharge flipflop

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IV. SIMULATION RESULTS

Fig 5 shows the snapshots of the waveforms for the flip-flop. The internal switching activity of CDFF at node is less when compared the other techniques. The waveforms flip-flop outputs are glitch-free when the input stays high.

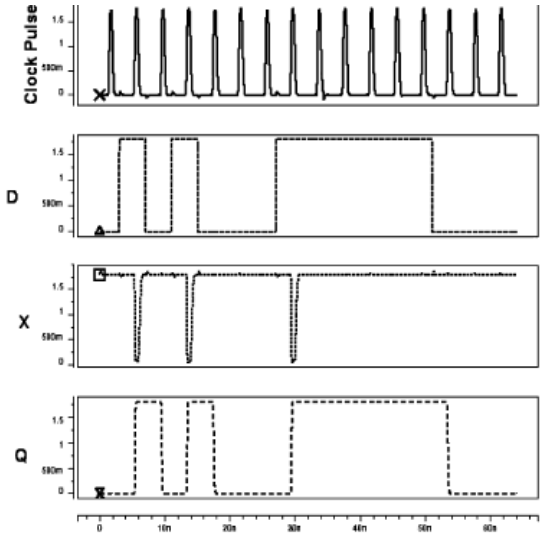

Fig. 5. Waveforms of conditional discharge flipflop

V. CONCLUSION

In this paper, a new technique, conditional discharge, is introduced to reduce the switching activity of some internal nodes flip-flops. This technique was utilized in a new Conditional discharge flipflop.

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