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A REVIEW OF LOW VOLTAGE AND LOW POWER CMOS ADDERS USING VLSI DESIGN IN VERILOG/VHDL

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Abstract - **The dominant portion of power dissipation in CMOS adder circuits, due to logic transitions, varies as the square of the supply, significant savings in power dissipation may be exacted by operating with reduced supply voltage. If the supply voltage is reduced while threshold voltage stays same, the noise margins will reduce. Addition is a crucial process because it usually involve carry ripple steps which must propagate a carry signal from each bit to it's higher bit position. This results in a substantial circuit delay. The adder which lies in the crucial delay path will effectively determine the system overall speed. To improve noise margins, the threshold voltages must also be made smaller. However sub-threshold leakage current increases exponentially when threshold voltage is reduced. The higher static dissipation may then offset the reduction in transitions portion of the dissipation. Hence the devices needed to have threshold voltages that maximizes the net reduction in the dissipation. Addition is an obligatory operation that is crucial to processing the fundamental arithmetic operations. Due to the potential versatility of adders in this contemporary research field, the existing adders and adder designs currently intended for future low voltage and low power environments. This can be achieved by the CMOS adders namely Parallel Adder, Ripple Carry Adder(RCA), Carry Look Ahead Adder(CLA), Carry Select Adder(CSL), Carry Save Adder(CSA), Carry Skip Adder(CSK), Conditional Sum Adder(COS).**

Keywords – **Parallel Adder, Ripple Carry Adder, Carry Look Ahead Adder, Carry Select Adder, Carry Save Adder, Carry Skip Adder, Conditional Sum Adder, Circuit Delay, Power Dissipation, Low Voltage, Low Power.**

I. INTRODUCTION

Low Power Design of VLSI circuits have been identified as critical technological need in recent years due to high demand for portable consumer electronic products. In this regard many innovative designs for basic logic functions using pass transistors and transmission gates have appeared in literature recently. These designs relied on the intuition and cleverness of the designers, without involving formal design procedures. Hence, a formal design procedure for realizing a minimal transistor CMOS pass network XOR-XNOR cell, that is fully compensated for threshold voltage drop in MOS transistors presented. This new cell can reliably operate within certain bounds when the power voltage is scaled down, as long as due consideration is given to the sizing of the MOS transistors during the initial design step. Low Power design is required to reduce the power in high-end systems with huge integration density and thus improve the speed of operation.

II. 4 BIT PARALLEL ADDER

A single full adder performs the addition of two one bit numbers and an input carry. But a Parallel Adder is a digital circuit capable of finding the arithmetic sum of two binary numbers that is greater than one bit in length by operating on corresponding pairs of bits in parallel. It consists of 4 full adders connected in a chain where the output carry from each full adder is connected to the carry input of the next higher order full adder in the chain. Parallel adders normally incorporate carry look ahead logic to ensure that carry propagation between subsequent stages of addition does not limit addition speed.

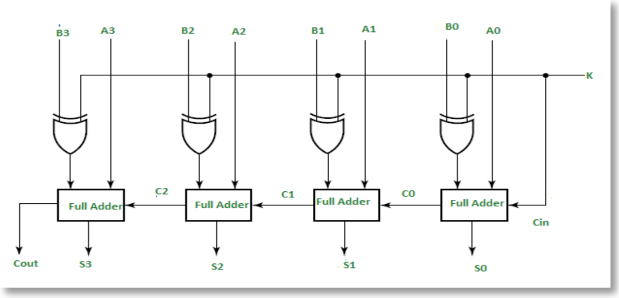


Fig.1 Logic Diagram of 4 Bit Parallel Adder

A) Boolean Equation of 4 Bit Parallel Adder:

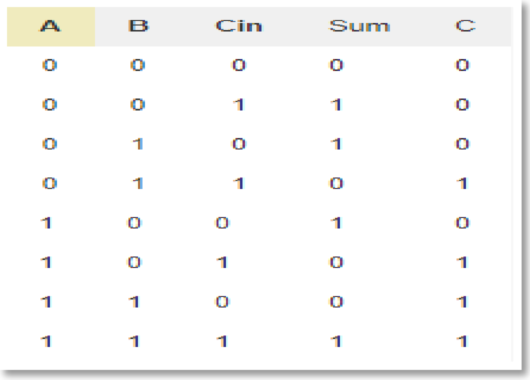
For the SUM (S) bit:

SUM = (A XOR B) XOR Cin = $(A \oplus B \oplus Cin)$

For the CARRY-OUT (Cout) bit:

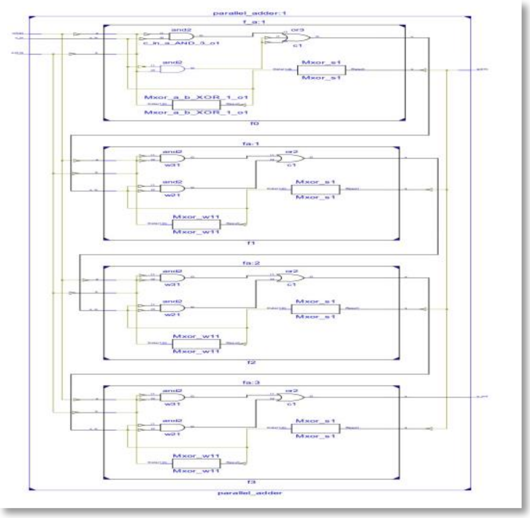
CARRY-OUT = (A AND B) OR (B AND Cin) OR (Cin AND A).

B) Truth Table of 4 Bit Parallel Adder

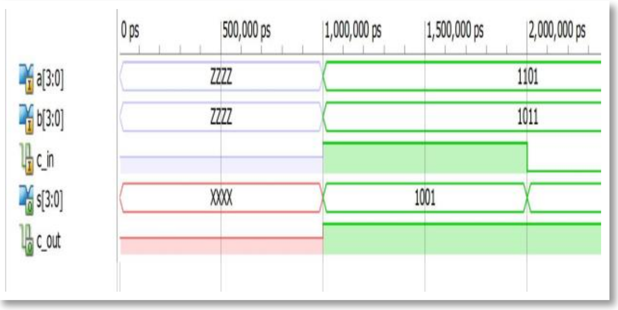


A	B	Cin	Sum	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

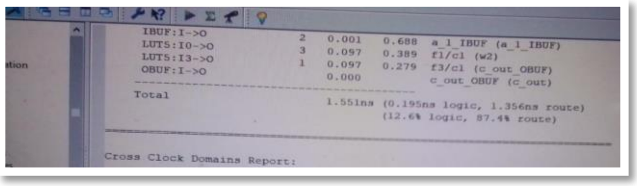
C) Gate level Design of 4 Bit Parallel Adder



D) Output of 4 Bit parallel Adder

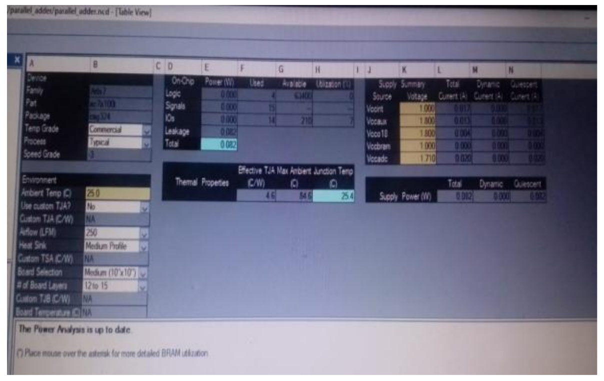


E) 4 Bit Parallel Adder’s Propagation Delay time simulated from synthesis report with XPower Simulation



```
    IBUF:I->O             2   0.001   0.688  a_1_IBUF (a_1_IBUF)
    LUT5:I0->O            3   0.097   0.389  f1/c1 (w2)
    LUT5:I3->O            1   0.097   0.279  f3/c1 (c_out_OBUF)
    OBUF:I->O                 0.000          c_out_OBUF (c_out)
    ----------------------------------------
    Total                     1.551ns (0.195ns logic, 1.356ns route)
                                      (12.6% logic, 87.4% route)

Cross Clock Domains Report:
```



/parallel_adder/parallel_adder.ncd - [Table View]

Device	
Family	Artix7
Part	xc7a100t
Package	csg324
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	4	63400	0
Signals	0.000	15	---	---
IOs	0.000	14	210	7
Leakage	0.082			
Total	0.082			

Supply Source	Summary Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.000	0.017	0.000	0.017
Vccaux	1.800	0.013	0.000	0.013
Vcco18	1.800	0.004	0.000	0.004
Vccbram	1.000	0.000	0.000	0.000
Vccadc	1.710	0.020	0.000	0.020

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	4.6	84.6	25.4

	Total	Dynamic	Quiescent
Supply Power (W)	0.082	0.000	0.082

The Power Analysis is up to date.

(*) Place mouse over the asterisk for more detailed BRAM utilization

III. 4 Bit Ripple Carry Adder (RCA)

The basic unit of Ripple Carry Adder is a full adder. It can be extended indefinitely to any number by connecting the carry-out of the previous 1-bit Full Adder to the carry-in of the next 1-bit Full Adder. Of all the adder architectures RCA offers good performance, nonetheless, its delay characteristics depend heavily on the length of the carry propagation path, thus making it a relatively unfavorable choice for circuits with nonrandom input operands. The worst-case delay increases linearly with the length of the carry propagation path, which depends on number of bits processed by operands, n. Also the area of the adder is proportional to n. Therefore in situations when high speed performance is crucial and the minimum amount of hardware is underperforming , using a RCA in an arithmetic operation would be detrimental. One of the most serious drawbacks of this adder is that each full adder has to wait for the carry out of the previous stage to output steady state result. Therefore even if the adder has a value at its output terminal, it has to wait for the carry before the output reaches a correct value. Generally speaking the worst-case delay of RCA is when a carry signal transition ripples through all stages of adder chain from the least significant bit to the most significant bit , which is approximated by,

t=(n-1)tc+ts

tc= Delay through the carry stage

ts= Delay through the sum stage

. **n= no of bits of full adder**

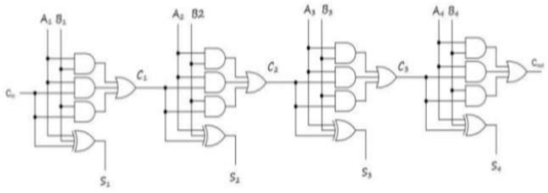
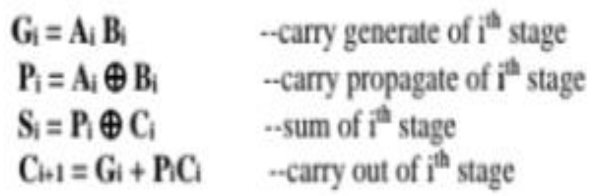


Fig.2 Logic Diagram of 4 Bit Ripple Carry Adder

A) Boolean Equation of 4 Bit Ripple Carry Adder



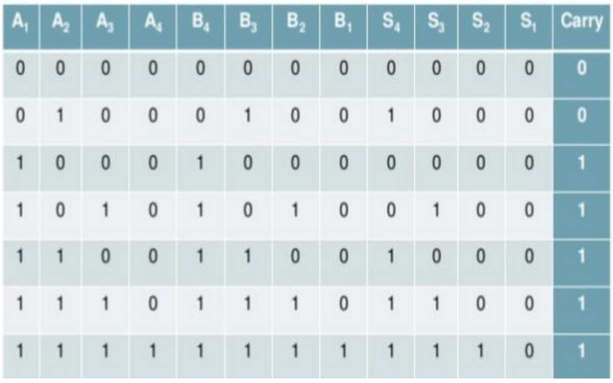
$G_i = A_i B_i$ --carry generate of ith stage

$P_i = A_i \oplus B_i$ --carry propagate of ith stage

$S_i = P_i \oplus C_i$ --sum of ith stage

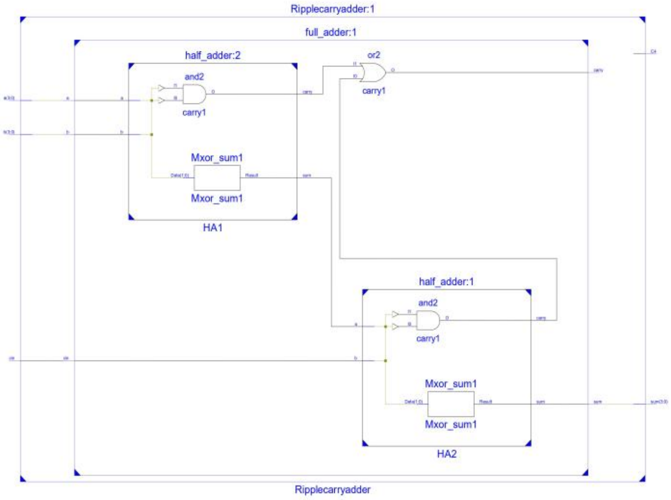
$C_{i+1} = G_i + P_i C_i$ --carry out of ith stage

B) Truth Table of 4 Bit Ripple Carry Adder

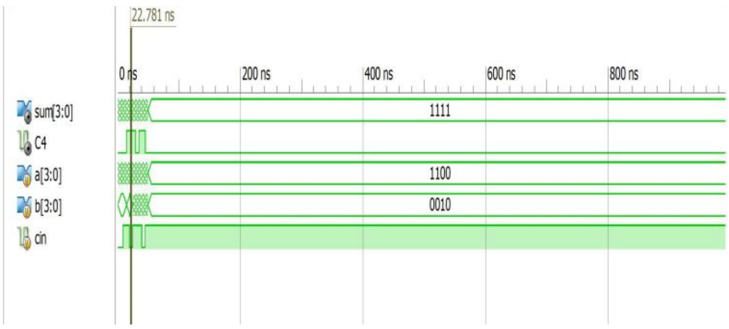


A_1	A_2	A_3	A_4	B_4	B_3	B_2	B_1	S_4	S_3	S_2	S_1	Carry
0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	1	0	0	1	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0	1
1	0	1	0	1	0	1	0	0	1	0	0	1
1	1	0	0	1	1	0	0	1	0	0	0	1
1	1	1	0	1	1	1	0	1	1	0	0	1
1	1	1	1	1	1	1	1	1	1	1	0	1

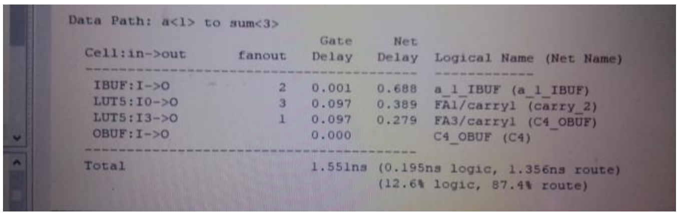
C) Gate Level Design of 4 Bit Ripple Carry Adder



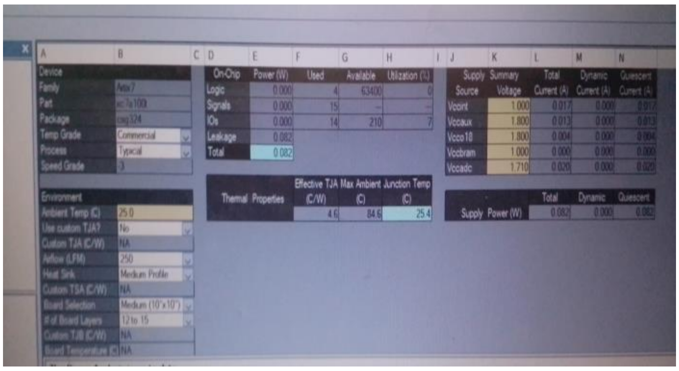
D) Output of 4 Bit Ripple Carry Adder



E) 4 Bit Ripple Carry Adder Propagation Delay time simulated from synthesis report with XPower Simulation



```
Data Path: a<1> to sum<3>
                                Gate      Net
  Cell:in->out        fanout   Delay    Delay   Logical Name (Net Name)
  ----------------------------------------   ------------
    IBUF:I->O              2   0.001    0.688   a_1_IBUF (a_1_IBUF)
    LUT5:I0->O             3   0.097    0.389   FA1/carry1 (carry_2)
    LUT5:I3->O             1   0.097    0.279   FA3/carry1 (C4_OBUF)
    OBUF:I->O                  0.000            C4_OBUF (C4)
  ----------------------------------------
  Total                        1.551ns (0.195ns logic, 1.356ns route)
                                        (12.6% logic, 87.4% route)
```



Device	
Family	Artix7
Part	xc7a100t
Package	csg324
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	4	63400	0
Signals	0.000	15	--	--
IOs	0.000	14	210	7
Leakage	0.082			
Total	0.082			

Supply Source	Summary Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.000	0.017	0.000	0.017
Vccaux	1.800	0.013	0.000	0.013
Vcco18	1.800	0.004	0.000	0.004
Vccbram	1.000	0.000	0.000	0.000
Vccadc	1.710	0.020	0.000	0.020

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	4.6	84.6	25.4

	Total	Dynamic	Quiescent
Supply Power (W)	0.082	0.000	0.082

IV. 4 Bit Carry Look Ahead Adder (CLA)

It is an adder with time propagation duration in O(log n) and whose area size requirement is in O(n log n). The delay time of CLA architecture therefore exhibits logarithmic dependency on the size of the adder, which allows the propagation delay of the carry signal to be minimized.

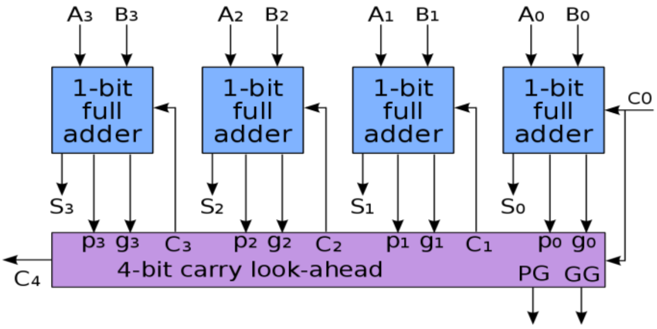


Fig.3 Logic Diagram of 4 Bit Carry Look Ahead Adder

Ci has to overcome 2 gates (AND & OR) in order to produce Ci+1.

Carry Propagate = 2n

n - number of bits.

For 4 bit adder n =4 ; therefore Carry Propagate = 8

It has to overcome **8 gate levels** to produce resultant carry.

The Propagate P and generate G in a full-adder, is given as:

Pi = Ai XOR Bi (Carry propagate**)**

Gi = Ai.Bi (Carry generate)

The new expressions for the output sum and the carryout are given by:

Si = Pi XOR Ci-1

Ci+1= Gi + PiCi

These equations show that a carry signal will be generated in two cases:

1) if both bits Ai and Bi are 1

2) if either Ai or Bi is 1 and the carry-in Ci is 1.

The general expression is

Ci+1= Gi + PiGi-1 + PiPi-1Gi-2 + ……. PiPi-1….P2P1G0 + PiPi-1 ….P1P0C0.

A) Boolean Equation of 4 Bit Carry Look Ahead Adder

Pi = Ai XOR Bi Carry propagate

Gi = Ai.Bi Carry generate

Si = Pi XOR Ci

Ci+1 = Gi OR Pi AND Ci

C0 - (1) to be given as an input

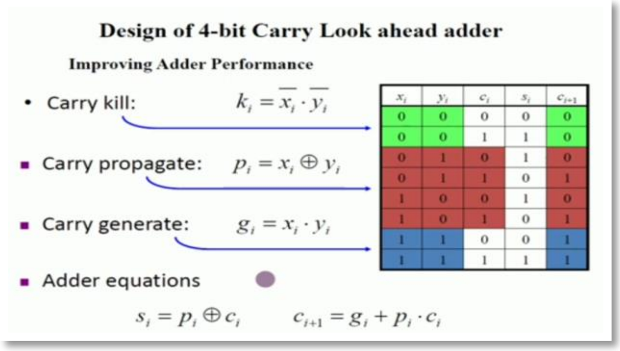
C1 = G0+P0.C0 -(2)

C2 = G1+P1.G0+P1.P0.C0 -(3)

C3 = G2+P2.G1+P2.P1.G0+P2.P1.P0.C0 -(4)

C4 = G3+P3.G2+P3.P2.G1+P3.P2.P1.G0+P3.P2.P1.P0.C0 -(5)

B) Truth Table of 4 Bit Carry Look Ahead Adder



Design of 4-bit Carry Look ahead adder

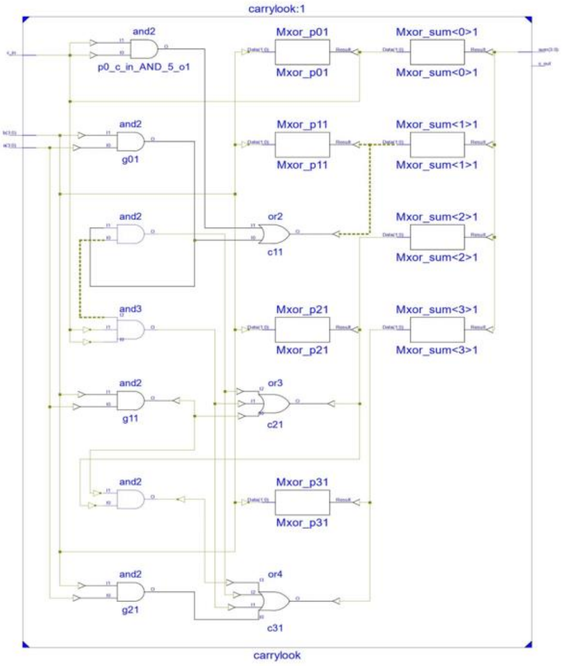
Improving Adder Performance

- Carry kill: $k_i = \overline{x_i} \cdot \overline{y_i}$
- Carry propagate: $p_i = x_i \oplus y_i$
- Carry generate: $g_i = x_i \cdot y_i$
- Adder equations

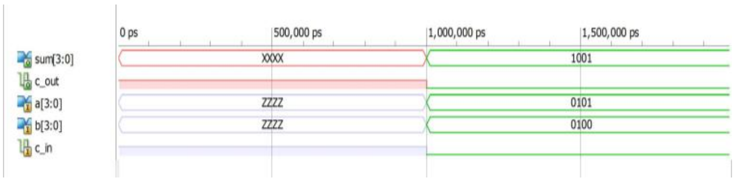
$s_i = p_i \oplus c_i \qquad c_{i+1} = g_i + p_i \cdot c_i$

x_i	y_i	c_i	s_i	c_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

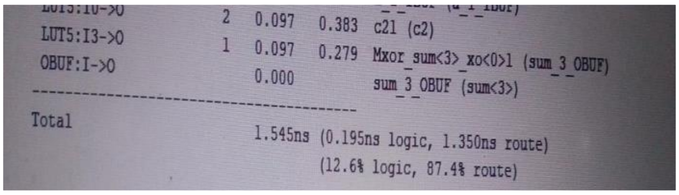
C) Gate Level Design of 4 Bit Carry Look Ahead Adder



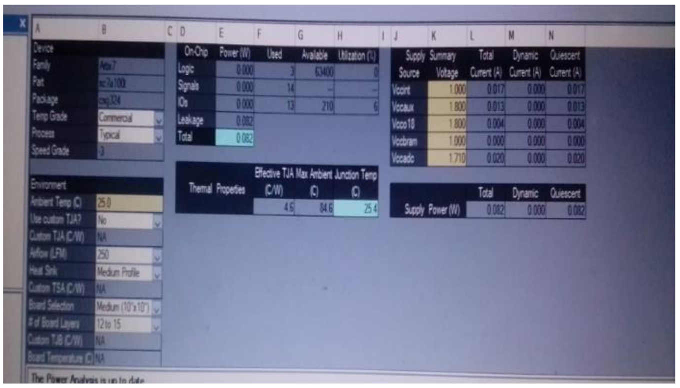
D) Output of 4 Bit Carry Look Ahead Adder



E) 4 Bit Carry Look Ahead Adder Delay time simulated from synthesis report with XPower Simulation



```
  LUT5:I0->O          2   0.097   0.383  c21 (c2)
  LUT5:I3->O          1   0.097   0.279  Mxor_sum<3>_xo<0>1 (sum_3_OBUF)
  OBUF:I->O               0.000          sum_3_OBUF (sum<3>)
 ----------------------------------------
 Total                    1.545ns (0.195ns logic, 1.350ns route)
                                  (12.6% logic, 87.4% route)
```



Device	
Family	Artix7
Part	xc7a100t
Package	csg324
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	3	63400	0
Signals	0.000	14	--	--
IOs	0.000	13	210	6
Leakage	0.082			
Total	0.082			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	4.6	84.6	25.4

Supply Source	Summary Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.000	0.017	0.000	0.017
Vccaux	1.800	0.013	0.000	0.013
Vcco18	1.800	0.004	0.000	0.004
Vccbram	1.000	0.000	0.000	0.000
Vccadc	1.710	0.020	0.000	0.020

	Total	Dynamic	Quiescent
Supply Power (W)	0.082	0.000	0.082

The Power Analysis is up to date

V. 4 Bit Carry Select Adder (CSL)

It is a particular way to implement an adder that computes (n+1) bit as a sum of two (n) bit numbers.CSL adder is simple but faster than other adders. In CSL both the n-bit operands Ai and Bi are divided into k blocks of possibly different sizes. The additional cost of the CSL over the RCA is the duplicate carry chain and the select logic. Then CSL adder using a multiplexer, depending on the real carryout, the correct sum is chosen. The delay of n-bit carry select adder based on an m-bit CLA blocks can be given by the following equation when using constant carry number blocks ,

T=t seup + m t carry + (n/m) t mux + t sum

And by the following equation when using successively incremented carry number blocks respectively,

T=t seup + m t carry +(2n)^0.5 t mux + t sum.

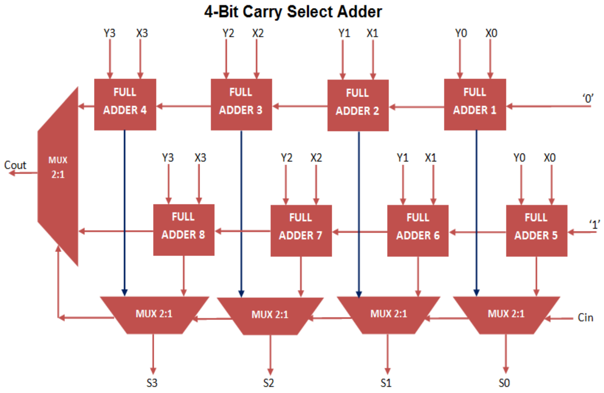
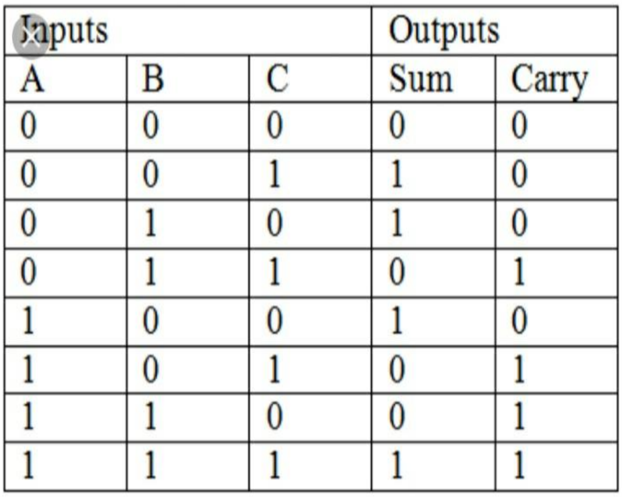


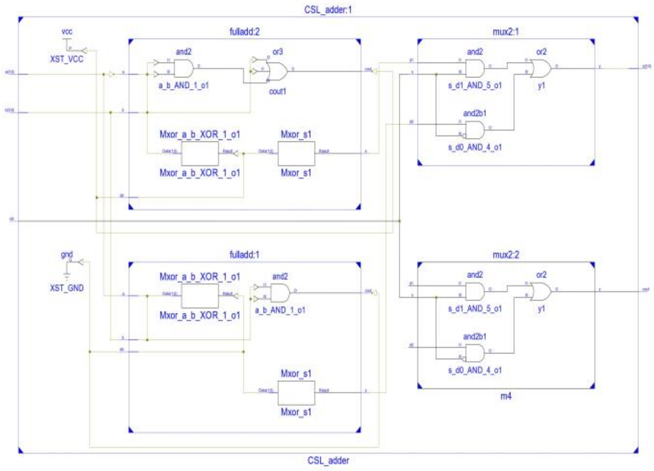
Fig. 4 Logic Diagram of 4 Bit Carry Select Adder

A) Truth Table of 4 Bit Carry Select Adder

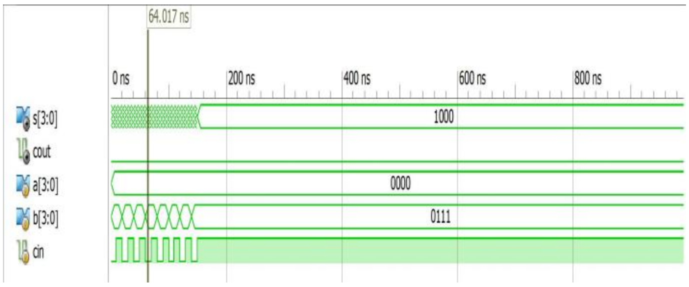


Inputs			Outputs	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

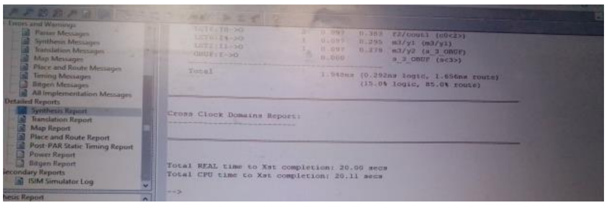
B) Gate Level Design of 4 Bit Carry Select Adder



C) Output of 4 Bit Carry Select Adder



D) 4 Bit Carry Select Adder Propagation Delay time simulated from synthesis report with XPower Simulation



```
    LUT6:I0->O        2   0.097   0.383  f2/cout1 (c0<2>)
    LUT6:I4->O        1   0.097   0.295  m3/y1 (m3/y1)
    LUT2:I1->O        1   0.097   0.278  m3/y2 (s_3_OBUF)
    OBUF:I->O             0.000          s_3_OBUF (s<3>)
    ----------------------------------------
    Total                 1.948ns (0.292ns logic, 1.656ns route)
                                  (15.0% logic, 85.0% route)

=========================================================================

Cross Clock Domains Report:
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=========================================================================


Total REAL time to Xst completion: 20.00 secs
Total CPU time to Xst completion: 20.11 secs

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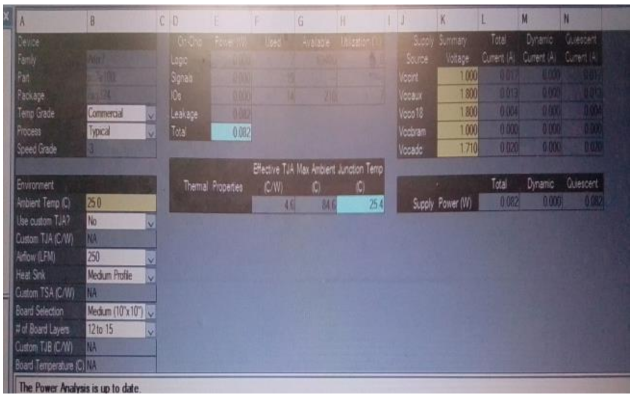


A	B
Device	
Family	Artix7
Part	xc7a100t
Package	csg324
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	7	63400	0
Signals	0.000	19	---	---
IOs	0.000	14	210	7
Leakage	0.082			
Total	0.082			

Supply Source	Summary Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.000	0.017	0.000	0.017
Vccaux	1.800	0.013	0.000	0.013
Vcco18	1.800	0.004	0.000	0.004
Vccbram	1.000	0.000	0.000	0.000
Vccadc	1.710	0.020	0.000	0.020

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	4.6	84.6	25.4

	Total	Dynamic	Quiescent
Supply Power (W)	0.082	0.000	0.082

The Power Analysis is up to date.

VI. 4 BIT CARRY SAVE ADDER (CSA)

A CSA tree consists of CSA operators and one adder at the root of the tree. The CSA operators are used to transform an arbitrary number of operands in the addition process to produce two adding operands, after which the adder at the root of the CSA tree computes final sum. Unlike RCA, CLA, CSL adders, the CSA realizes the concurrent addition of multiple operands, which is a basic requirement of multiplication. Instead of using the 2-operand adders that necessitate the time consuming carry propagation to repeat several times, depending on the number of operands, the CSA's timing could be improved with a little increase or even a reduction in area. Time to obtain Summation is given by,

T = (k-2) AND Tcsa OR Tcpa.

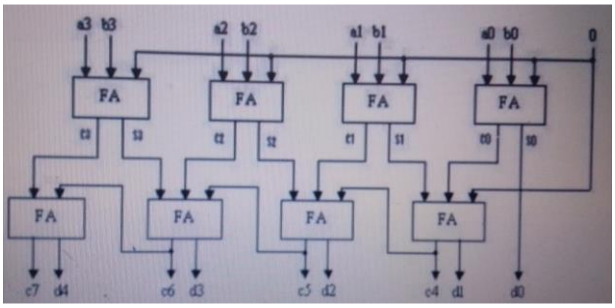


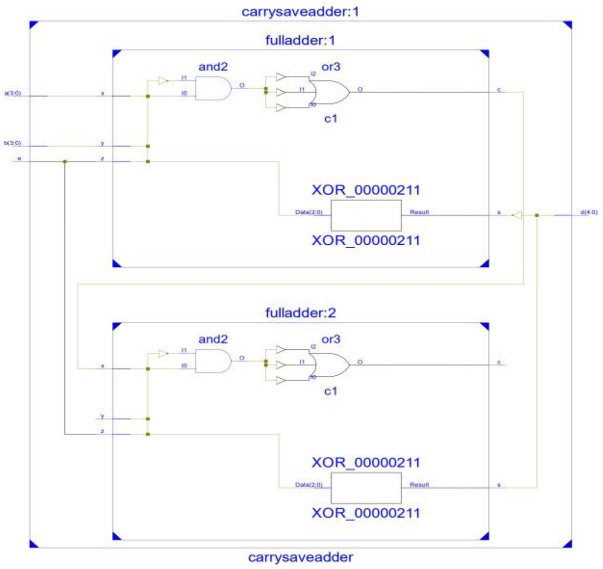
Fig.5 Logic Diagram of 4 Bit Carry Save Adder

A) Boolean Equation of 4 Bit Carry Save Adder

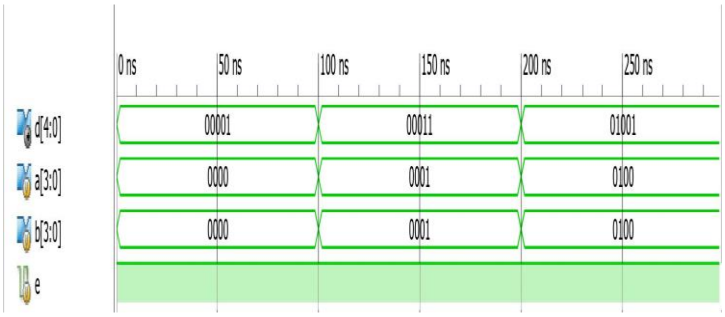
SUM = (A XOR B) XOR Cin = (A ⊕ B ⊕ Cin)

CARRY-OUT = (A AND B) OR (B AND Cin) OR (Cin AND A).

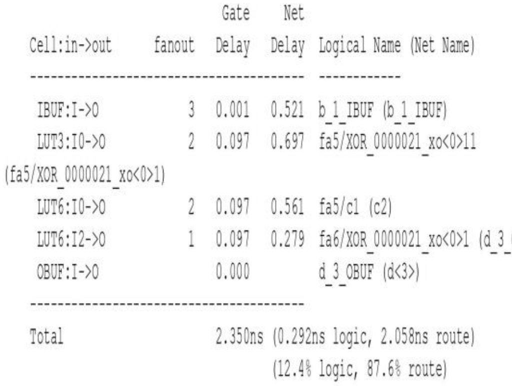
B) Gate Level Design of 4 Bit Carry Save Adder



C) Output of 4 Bit Carry Save Adder

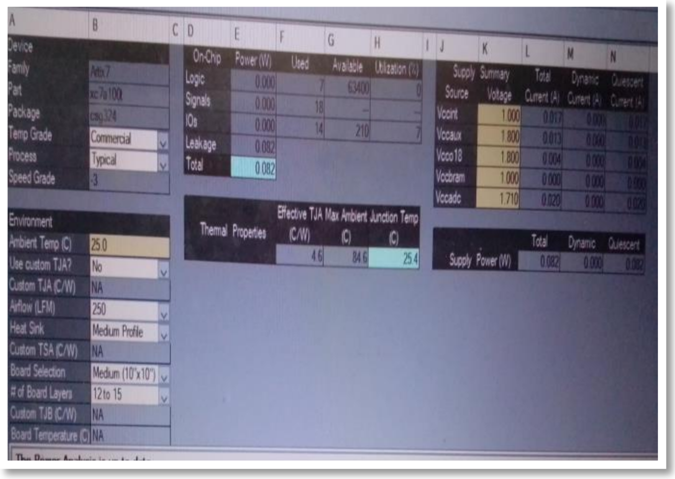


D) 4 Bit Carry Save Adder Propagation Delay time simulated from synthesis report with XPower Simulation



```
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             3   0.001   0.521  b_1_IBUF (b_1_IBUF)
     LUT3:I0->O            2   0.097   0.697  fa5/XOR_0000021_xo<0>11
(fa5/XOR_0000021_xo<0>1)
     LUT6:I0->O            2   0.097   0.561  fa5/c1 (c2)
     LUT6:I2->O            1   0.097   0.279  fa6/XOR_0000021_xo<0>1 (d_3_OBUF)
     OBUF:I->O                 0.000          d_3_OBUF (d<3>)
    ----------------------------------------
    Total                      2.350ns (0.292ns logic, 2.058ns route)
                                       (12.4% logic, 87.6% route)


=========================================================================
```



Device	
Family	Artix7
Part	xc7a100t
Package	csg324
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	7	63400	0
Signals	0.000	18	---	---
IOs	0.000	14	210	7
Leakage	0.082			
Total	0.082			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	4.6	84.6	25.4

Supply Source	Summary Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.000	0.017	0.000	0.017
Vccaux	1.800	0.013	0.000	0.013
Vcco18	1.800	0.004	0.000	0.004
Vccbram	1.000	0.000	0.000	0.000
Vccadc	1.710	0.020	0.000	0.020

	Total	Dynamic	Quiescent
Supply Power (W)	0.082	0.000	0.082

VII. 4 Bit Carry Skip Adder (CSK)

A CSK adder is similar to how the MCC adder works, which is to reduce the carry propagation time by skipping over groups of successive adder stages.In general, with the assumption that the delay of the skip logic is equal to the carry propagation delay from one stage to another , the overall time of the carry propagation chain is calculated as follows,

T carry = (K-1) + (n/K - 2) + (K-1) stages.

K refers to an n-bit CSK with fixed block size.

The design of Carry Skip Adder that achieves low power dissipation and high performance operation. The CSK adder's delay and power dissipation are reduced by dividing the adder into variable-sized blocks that balance the delay of inputs to carry the chain . This grouping active power by minimizing extraneous glitches and transitions.

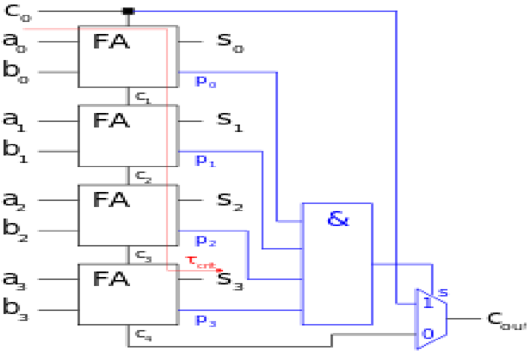


Fig.6 Logic Diagram of 4 Bit Carry Skip Adder

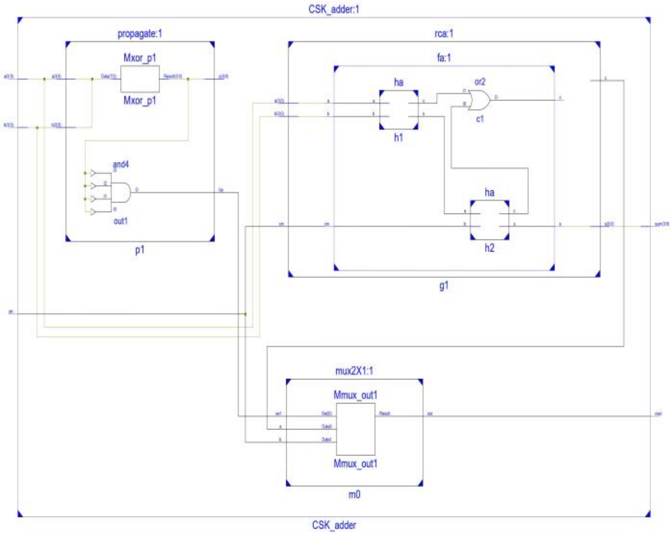
A) Boolean Equation of 4 Bit Carry Skip Adder

Pi = Ai XOR Bi

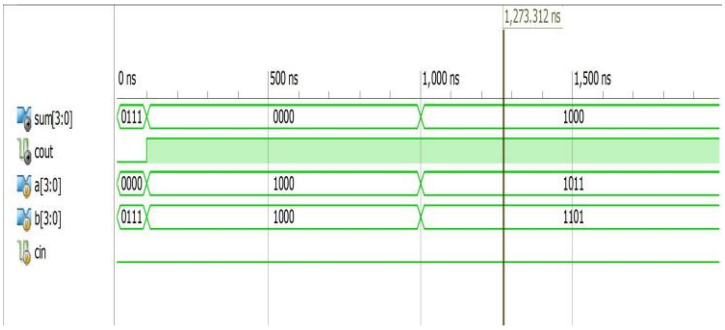
Si = Pi XOR Ci

Ci+1 = (Ai AND Bi)OR(Pi AND Ci)

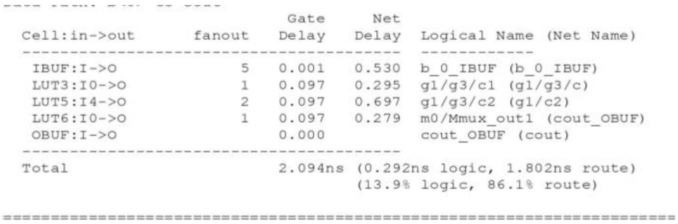
B) Gate Level Design of 4 Bit Carry Skip Adder



C) Output of 4 Bit Carry Skip Adder

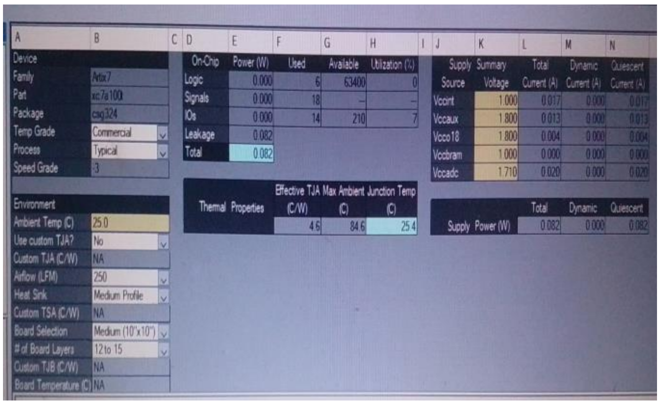


D) 4 Bit Carry Skip Adder Propagation Delay time simulated from synthesis report with XPower Simulation



```
                                Gate     Net
  Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   IBUF:I->O             5   0.001   0.530  b_0_IBUF (b_0_IBUF)
   LUT3:I0->O            1   0.097   0.295  g1/g3/c1 (g1/g3/c)
   LUT5:I4->O            2   0.097   0.697  g1/g3/c2 (g1/c2)
   LUT6:I0->O            1   0.097   0.279  m0/Mmux_out1 (cout_OBUF)
   OBUF:I->O                 0.000          cout_OBUF (cout)
  ----------------------------------------
  Total                      2.094ns (0.292ns logic, 1.802ns route)
                                     (13.9% logic, 86.1% route)

==================================================================
```



A	B
Device	
Family	Artix7
Part	xc7a100t
Package	csg324
Temp Grade	Commercial
Process	Typical
Speed Grade	-3
Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	6	63400	0
Signals	0.000	18	---	---
IOs	0.000	14	210	7
Leakage	0.082			
Total	0.082			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	4.6	84.6	25.4

Supply Source	Summary Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.000	0.017	0.000	0.017
Vccaux	1.800	0.013	0.000	0.013
Vcco18	1.800	0.004	0.000	0.004
Vccbram	1.000	0.000	0.000	0.000
Vccadc	1.710	0.020	0.000	0.020

	Total	Dynamic	Quiescent
Supply Power (W)	0.082	0.000	0.082

VIII. 4 Bit Conditional Sum Adder (COS)

The underlying principle of this architecture is the parallel computation of two sets of conditional sums and conditional carries for each bit position. To minimize the computation time, the given 'n' bits are divided into smaller groups so that the serial carry propagation within the groups can be carried out in parallel. The COS approach is very similar to CSL. The major difference is that in COS the division of the n bits into sub-blocks continues until the extreme of having only single-bit adders if n is an integer power of 2. The COS scheme can still be implemented even if n is not a power of 2 because sub-blocks of equal sizes are not compulsory.

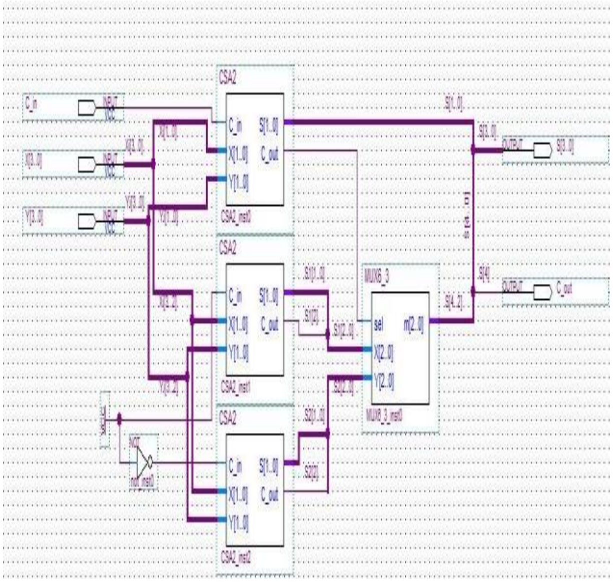


Fig. 7 Logic Diagram of 4 Bit Conditional Sum Adder

A) Boolean Equation of 4 Bit Conditional Sum Adder

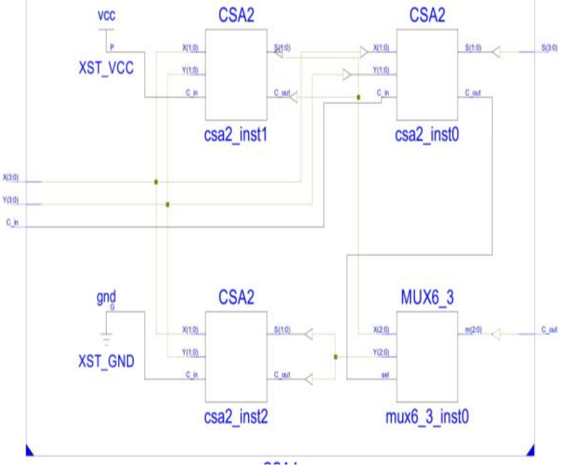
$$S_i^0 = A_i \oplus B_i$$

$$C_{i+1}^0 = A_i \bullet B_i$$

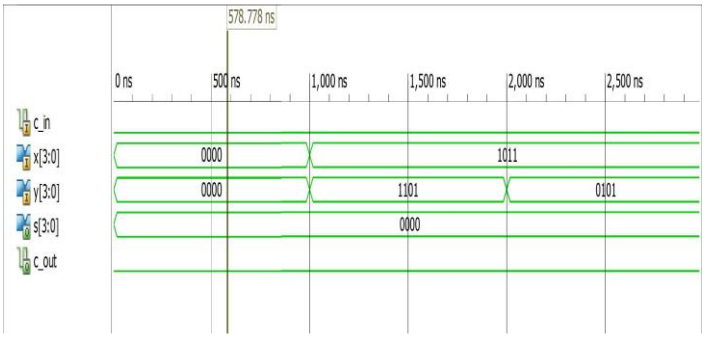
$$S_i^1 = \overline{A_i \oplus B_i}$$

$$C_{i+1}^1 = A_i + B_i$$

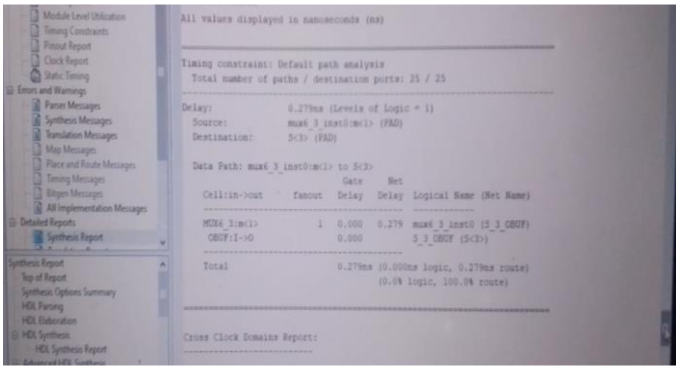
B) Gate Level Design of 4 Bit Conditional Sum Adder



C) Output of 4 Bit Conditional Sum Adder



D) 4 Bit Conditional Sum Adder Propagation Delay time simulated from synthesis report with XPower Simulation



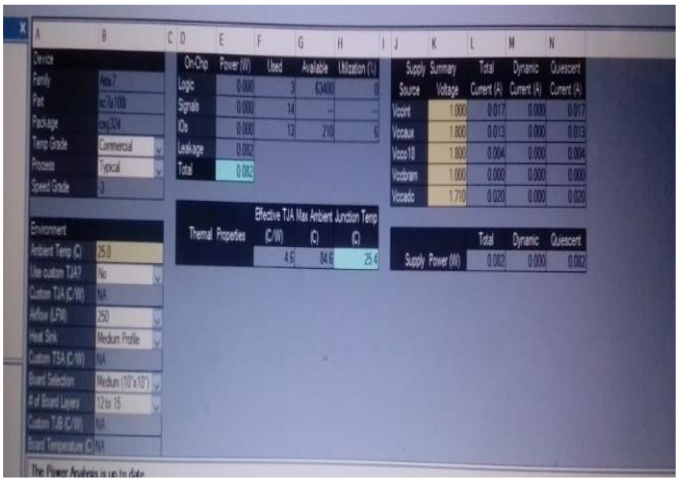
```
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 25 / 25
-------------------------------------------------------------------------
Delay:               0.279ns (Levels of Logic = 1)
  Source:            mux6_3_inst0:m<1> (PAD)
  Destination:       S<3> (PAD)

  Data Path: mux6_3_inst0:m<1> to S<3>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     MUX6_3:m<1>           1   0.000   0.279  mux6_3_inst0 (S_3_OBUF)
     OBUF:I->O                 0.000          S_3_OBUF (S<3>)
    ----------------------------------------
    Total                      0.279ns (0.000ns logic, 0.279ns route)
                                       (0.0% logic, 100.0% route)

=========================================================================

Cross Clock Domains Report:
--------------------------
```



Device	
Family	Artix7
Part	xc7a100t
Package	csg324
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	3	63400	0
Signals	0.000	14	---	---
IOs	0.000	13	210	6
Leakage	0.082			
Total	0.082			

Supply Source	Summary Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.000	0.017	0.000	0.017
Vccaux	1.800	0.013	0.000	0.013
Vcco18	1.800	0.004	0.000	0.004
Vccbram	1.000	0.000	0.000	0.000
Vccadc	1.710	0.020	0.000	0.020

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	4.6	84.6	25.4

	Total	Dynamic	Quiescent
Supply Power (W)	0.082	0.000	0.082

The Power Analysis is up to date

IX. Performance Evaluation of CMOS Adders

An overall performance evaluation and comparison, to rank the adders has been carried out based on 1.2 micro-meter CMOS technology.

LOGIC STYLE	INPUT BIT	AVERAGE INPUT VOLTAGE (V)	AVERAGE INPUT POWER (W)	PROPAGATION DELAY (ns)
Parallel Adder	4 Bit	1.7	0.082	1.551
Ripple Carry Adder	4 Bit	1.7	0.082	1.55
Carry Look Ahead Adder	4 Bit	1.7	0.081	1.545
Carry Select Adder	4 Bit	1.7	0.086	1.948
Carry Save Adder	4 Bit	1.7	0.082	2.350
Carry Skip Adder	4 Bit	1.7	0.082	2.094
Conditional Sum Adder	4 Bit	1.7	0.080	0.279

Fig.8 Performance Comparison of Different Logic Style CMOS Adders.

X. Conclusion

CMOS Adders [Parallel Adder, RCA Adder, CLA Adder, CSL Adder, CSA Adder, CSK Adder, COS Adder] has been analyzed which exhibits a higher speed and lower power consumption compared with those of the conventional one. Delay, Power and area are the constituent factors in VLSI design that limits the performance of any circuit. The proposed design of all the CMOS Adders were simulated and synthesized in Xilinx ISE 14.7 and the source code is written in Verilog / VHDL, and the Power analysis is simulated in X Power Analysis. Since the conditional sum adder deals with carry generation and sum generation separately, and the carry propagation is performed faster than the sum propagation, its operation speed can be improved with a propagation delay of 0.279 ns with a power consumption of 0.080 watts. The speed enhancement was achieved by modifying the structure through the complementary transmission gate logic. The static and dynamic power dissipation in CMOS Adders were minimized by VLSI design. The Propagation Delay has been reduced and thus Performance characteristics for these adders are tabulated.

XI. REFERENCE

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