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LOW-POWER HIGH-PERFORMANCE CARRY SKIP ADDER: A REVIEW

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***Abstract*: The delay of a ripple carry adder is upgraded by using a carry skip adder (CSKA) with much less effort as compared to other adders because it has low power-delay product. It contains blocks of full adders that are combined together and whose combination generally influences the overall speed of CSKA. Carry skip adders synthesized using different techniques are reviewed in this paper. For the skip logic, we can use the AND-OR Invert (AOI) compound gates or we can simply use a multiplexer.**

I. INTRODUCTION

As the demand for mobile electronic devices keeps increasing, power productive VLSI circuits are needed for fulfilling the need. For faster computations, these devices should use low power and less area consuming circuits that also have better speed. Adder is the very basic component of a processor as addition is the fundamental arithmetic operation. Adders are fundamental blocks in ALUs. There have been several works done to optimize the power and the speed of CSKA which are mentioned later in this paper. It is required to get better speeds with minimum power dissipations and that presents a challenge to the VLSI designers.

A very effective technique to lessen power dissipation of a circuit is to bring down the supply voltage. And because the switching energy depends very much on the voltage, power consumption is effectively reduced. Presently, we have numerous adders having various delays and power dissipations. For example, RCA (ripple carry adder), CIA (carry increment adder), carry skip adder (CSKA), and parallel prefix adder (PPA) (Islam, Rahman, Begum and Hafiz, 2009). The simplest of them is RCA as it has the least area and the least power dissipation yet it has the highest delay. Then comes the Carry Select Adder which has power dissipation, the speed and the utilizes area usage somewhat bigger than that of RCA. Carry look-ahead adders produce the carry quicker than all of the other adders. Carry skip adder is a proficient adder when it comes to area usage and power consumption. It increases the speed of addition by propagating a carry bit around a whole adder. The delay given by CSKA is much less than that given by RCA, but its power consumption and area is similar to RCA. CSKA causes wide attention because of its high computing efficiency and short delay. Also, because of small number of transistors, carry skip adder has very short length of wirings and also a simple layout.

The contribution of the paper is as under:

- Different types of carry skip adders are reviewed.
- Different carry skip logics are compared by clearly mentioning their advantages and disadvantages.

The rest of the paper is organized as follows:

In section I, Introduction of carry skip adder and several other adders is presented. In section II, literature survey is presented. Section III contains limitations of the existing system. In section IV, comparisons and discussions are there. Section V contains the conclusion of the paper.

II. LITERATURE SURVEY

Small electronic devices have become an essential part of human life. Devices which have very high speed and consume less power are high in demand. The main problem while designing the high speed arithmetic units is reducing the time that should be allowed for the propagation of carry in the adders. Many solutions have been proposed for this problem. One of them is using carry skip adder instead of any other adder as it forms the basic component present in any processor.

2.1 Carry Skip Adder Using Blocks of Full Adders

The carry skip adder (CSKA) was proposed for the first time by Lehman et al. (1961). Its speed was found to be more than the conventional RCA. Some programs are implemented to carry out the minimization of latencies in carry skip adders. Algorithms are presented in T language. A CSKA contains blocks of full adders combined together which affects the overall speed of CSKA (Chan, Schlag, Thomborson and Oklobdzija, 1992). The paper configures CSKA and CSLA adders to attain minimum latency.

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Many strategies have been proposed over time to minimize the delay of full adders in blocks. (Tale and Deshmukh, 2018).

2.2 Carry Skip Adder using Concatenation and Incrementation Schemes

M. Bahadori et al. (Bahadori, Kamal, Afzali, Pedram, 2016) represents a structure of CMOS CSKA that exhibits lower energy consumption and a higher speed as compared to the conventional one. Here, carry skip logic is achieved by using OR-AND-Invert (OAI) and AND-OR-Invert (AOI) compound gates instead of multiplexer logic. The speed is also enhanced by using concatenation and incrementation schemes.

2.3 Carry Skip Adder using Efficient Full Adders

In most of the VLSI applications, delay, power, and area are the most important points that should be considered. This can be achieved by having a fast adder. Comparison has been done between various adders in which it is found that Carry-skip adder dissipates more power and consumes more area when compared to RCA but have less delay. So, the problem of power and area is overcome by using efficient full adders in the paper presented by S. K. Shirakol et al. (Shirakol, Kulkami, Akash, Parvati, 2014)

2.4 Carry Skip Adder using Pass Transistor Logic

P. P. Patil et al. (Patil and Hatkar, 2016) presented a method to improve the overall speed performance of a CSKA, where, the optimization technique is used in the case of constant block size. The optimization technique used here is the pass transistor logic. When compared, Pass Transistor Logic consumes less power than CMOS technique. Also, PTL technique is good in case of variation in supply voltages than CMOS technique. If the temperature is varied, PTL technique again gives better Power Delay Product (PDP) than CMOS technique.

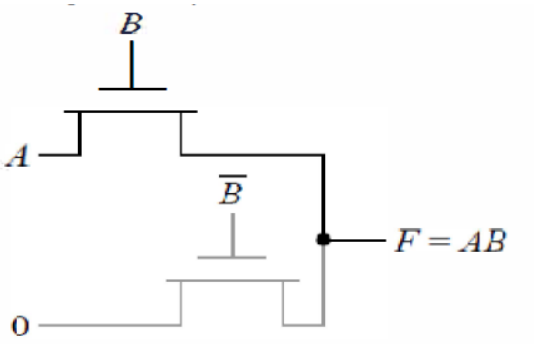

Fig. 1. AND gate using Pass Transistor Logic

2.5 Carry Skip Adder using Reversible Logic

Reversible logic is very important in various fields like low power designs using CMOS, DSP (digital signal processing) etc. Another advantage of using reversible logic is that it does not dissipate heat since it only executes the functions having one-to-one links between the outputs and the inputs.

A. K. Biswas et al. (Biswas, Hasan, Hasan, Chowdhury and Babu, 2008) designed a BCD adder and a BCD adder having carry skip operation utilizing the reversible logic. Furthermore, the modified designs are better as far as delay, area required and number of trash output created.

M. S. Islam et al. (Islam, Rahman, Begum, Hafiz, 2009) designed fault tolerant carry skip adders using reversible logic. The design here is optimized in terms of gate count, garbage outputs, and hardware complexity.

Y. Pang et al. (Pang, Wang and Wang, 2012) designed another CSKA having 16 bit inputs outlined using reversible logic. It turns out to be advantageous because of low delay and low power dissipation.

2.6 Variable Stage Carry Skip Adder

A CSKA using 90nm technology of CMOS is simulated. Here, the adder has 7 stages and is designed on Cadence Virtuoso. Variable stage and fixed stage CSKA configurations are analyzed and 16-bit high speed variable stage CSKA is proposed in which first and last stages are of 1 bit each and the size of stage increases until we reach the middle stage (the bulkiest one). Where, the middle stage here is named as the nucleus stage. The proposed structure reduces the power consumption by 8% and the delay by 61.75%. This has been proposed by A. Arora et al. (Arora and Niranjan, 2017).

I. Singh et al. (Singh and Dhingra, 2015) designed another CSKA and implemented it on Cadence Virtuoso in stages of 2, 8, 32 bits. A comparison is shown between CSKA having 8 bit input and RCA having 8-bit input in terms of delay and power dissipation. Power dissipated by CSKA is more than RCA whereas the delay is less.

Another efficient CSKA is designed by R. Abhinaya et al. (Abhinaya, Gayathri, Atchaya, Kumar and Balaji, 2019) using tanner eda tool and Xilinx software and the results are compared.

III. EXISTING SYSTEM

Conventional CSKA

The carry skip adder summarizes the comparison between CSLA and RCA. CSKA splits words that are added into the blocks. All the blocks has a RCA that generates the carry and the sum. Because of the carry computations, CSKA minimizes the delay by skipping the group of Full Adder stages.

- When all the bits of all inputs are dissimilar, Ai#Bi, we don't require to figure new estimation of carry for that same block, the input carry of

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that block is sent straightforwardly to the next block.

- Carry is generally propagated to the output of the block when the inputs are both 1, i.e. Bi=1 and Ai=1.
- Also, carry is not generated when the inputs are 0.

That's when we use CSKA to detect the input carry bit so that the block can be skipped.

Fig. 2. shows the schematic architecture of 8 bit Carry-skip adder.

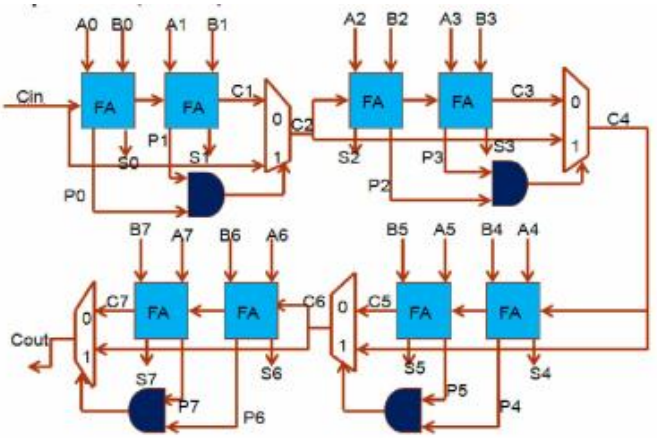

Fig. 2. Architectural block of 8-bit CSKA

Skip operation of CSKA is carry out by using multiplexers and AND gates as shown in the figure 1. Therefore, each stage in this structure consists of a RCA block and a skip logic.

A CSKA can be executed utilizing Fixed Stage Size (FSS) and also the Variable Stage Size (VSS) structures yet the most elevated speed is acquired utilizing VSS structure (Alioto and Palumbo, 2003) (Turrini, 1989).

In the existing system, the skip logic is implemented using multiplexers and AND gates. These multiplexers have large number of transistors that give us delays. Also, these systems have a large area coverage as they are implemented using 90 nm or 180 nm CMOS technologies.

IV. DISCUSSIONS AND FUTURE SCOPE

In this paper, different methods to improve the delay and reduce the power consumption of carry skip adder are discussed.

The results are different for the different papers. Sometimes, when the power consumption is low, the delay is high. And sometimes, when the delay is low, the power consumptions are high. So, to conclude, we can say that the incrementation and concatenation schemes used by M. Bahadori et al. (Bahadori, Kamal, Afzali, Pedram, 2016) and the pass transistor logic used by P. P. Patil et al. (Patil and Hatkar, 2016) are by far the best techniques to reduce both the power dissipation and the delay.

Authors	Publication Year	Technology Used (nm)	Parameters		Bits
			Power Consumption (µW)	Delay (ps)	
A. Arora	2017	90	0.00707	35.2	16
M. Bahadori	2016	45	-	-	-
P. P. Patil	2016	32	4	102.12	8
I. Singh	2015	NA	103.6	NA	8
K. Chirca		130	786	12.9	32
S. K. Shirakol	2014		0.73	0.041	16

V. CONCLUSION

When Carry Skip Adder is compared with other adders, like the Ripple Carry Adder, it consumes more power and more area. But the delay is always less as compared to Ripple Carry Adder. Hence, to overcome these limitations, the conventional circuit of Carry Skip Adder is slightly modified by using different techniques and their comparison is presented.

VI. ACKNOWLEDGEMENT

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