International Journal of Engineering Applied Sciences and Technology, 2020
Vol. 5, Issue 3, ISSN No. 2455-2143, Pages 363-367
Published Online July 2020 in IJEAST (http://www.ijeast.com)

STUDY ON DIGITAL DOWN CONVERSION TECHNIQUE IMPLEMENTED ON FPGA

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***Abstract*— The objective of this paper is to study the literature for FPGA based digital sown conversion technique for radars. The review of literature describes work done in the field of Radar technology. Elaborates the step by step improvements in the field of waveform generation and processing technology equipped in digital receivers. Radar technology primarily in the area of military applications is in an unceasing process of extending its capabilities. Phased array radars add to this process as it was initially invented for use in military radar systems to steer a beam of radio waves quickly across the sky to detect planes and missiles. High speed analog to digital converts employed in digital receivers digitize the received signal. The digitized signal is then down converted using digital signal processing techniques to obtain I and Q baseband signals. Basically, the signal is sampled by A/D converter, frequency shifted to baseband, low-pass filtered and decimated to produce I and Q digital data. The importance of how FPGA with a large RAM capacity provides an adequate storage for pulse width of most radar applications and high clock rates allows generation of high bandwidth waveform to enable greater radar resolution is described.**

Keywords— **Digital down conversion, Phased array radars, FPGA, Direct digital synthesizer.**

I. INTRODUCTION

The word "radar" is the abbreviation for "Radio Detection and Ranging" which is defined as the art of detecting target presence, determining its direction and distance and recognizing its character via radio waves. In modern radar design, phased array radar is very important and technology forming multiple electronic beams is the most important technology in a phased array radar. Phased array is an array of antennas within which the relative phases of the several signals feeding the antennas are varied in such a simplest way that the effective radiation pattern of the array is reinforced in a very desired direction and suppressed in undesired directions.[1] The echo that is received from radar is then processed by waveform processing unit which is implemented on FPGA based hardware. Modern day high density FPGAs are best suited for implementing these functionalities as they provide high computational bandwidth. Also FPGA provides better performance with improved Spurious-Free Dynamic Range (SFDR); faster processing and inbuilt reconfigurabilty; reduction in power requirement, increased precision performance; excellent quadrature channel phase balance, increased temperature stability. The digital receiver consisting of analogue to digital converter is capable of digitizing the received signal. The digitized signal is down converted to I and Q baseband signal using digital processing techniques. The down converted signal is then passed through a low pass filter and decimated. This process helps gather knowledge about the interested data which is the overriding doppler

II. REVIEW OF LITERATURE

Shaya Karimkashi et al.[5] (2013) -"Cylindrical Polarimetric Phased Array Radar Demonstrator: Design and Analysis of a Frequency Scanning Antenna Array" presents the design, modelling and measurement results of a mid-size cylindrical polarimetric phased array radar. The author explains how beam scanning in the elevation is obtained using the frequency scanning concept while the azimuth scanning is achieved using both the commutation and the beam scanning. The antenna array operating at a frequency range of 2.7 GHz to 3 GHz consisting of 96 vertical column mounted on the surface of the cylinder was designed and modelled. A Taylor amplitude distribution was applied to a 19-element vertical linear array antenna and low sidelobe levels were obtained for both horizontal and vertical polarizations. It was shown that using multilayer microstrip technology resulted in very low cross polarization patterns. In addition, a very good isolation between the horizontal and vertical port was achieved.

Phased array technology has been evolving steadily with advances in solid-state microwave integrated circuits, analysis and design tools and reliable fabrication practices. The paper [6](2015) - "The Evolution of Modern Phased Array Architectures" explains that the next- generation phased arrays will employ high levels of digitization, enabling a wide range of capacity and performance improvements. The authors implement tile array architecture, which greatly reduces the number of printed circuit boards and connectors in the array, substantial cost reductions are also achieved. Explaining the tile architecture the authors gives a cost comparison between slat architecture and tile architecture. The comparison greatly

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signify that tile architecture is better in terms of cost than slat architecture. The rapid evolution of digital processor technology foster the emergence of fully digital arrays, with significant improvements in performance. The use of solid-state microwave integrated circuits have enabled the widespread use of phased arrays in military systems, but the cost remains high. In this paper the authors proposed a design using high-volume commercial microwave manufacturing techniques which has the potential to dramatically lower the cost of phased arrays.

TABLE I: COST CONSIDERATION OF SLAT AND TILE ARCHITECTURE [6]

Component	Slat($/m^2)	Tile ($/m^2)
T/R chip set	$80,000	$80,000
Die handling	$40,000	N/A
T/R module packages	$400,000	$8000
RF boards	$150,000	$25,000
Cables & connectors	$10,000	$1,562
cooling	$180,000	$40,000
structure	$50,000	$16,250
Assembly & test	$80,000	$12,500
Total	$990,000/m^2	$183,312/m^2

An improved design method for a digital down converter (DDC) is proposed in paper [7] (2012)- "A Highly Efficient Digital Down Converter in Wide Band Digital Radar Receiver". The proposed design by authors satisfy the increased requirements for miniaturization and low power consumption of signal processor in the digital wide band radar receiver. With this structure the resource utilization and digital signal complexity are both reduced significantly. compared to conventional development methods, FPGA based design results show that logical resources are saved by 83.6% and power consumption is reduced by 110mW, which shows the reliability and good engineering applicability of this process. Adopting the sampling technique that the system sampling frequency is 4 times as high as the intermediate frequency of the input signal and employment of half band FIR filters, the improved design method can save a large amount of logical resources, especially multiplier blocks.

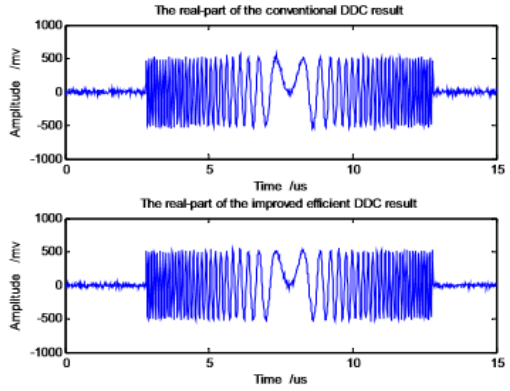

Figure 1:Comparison of conventional and improved DDC results.[7]

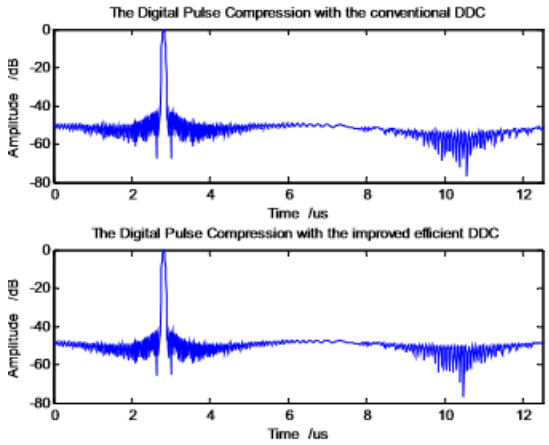

Figure 2: Comparison of digital pulse compression results[7]

Yogesh P Sajjan et al.[8](2015) - "FPGA Based Digital Beam Forming for Phased Array Radar" describes a method to achieve digital beam forming in transmitter section. The authors describe the system by designing a sixteen channel direct – digital waveform synthesizer using direct digital synthesizer (DDS) to enable digital beam steering of the transmitting side for a 4x4 array patch antenna. Each antenna element has a separate beam forming exciter. DDS is a digitally controlled method of generating signals whose frequency, phase and amplitude are controlled by the respective description words. Also how the hardware is implemented in FPGA is mentioned. The DDS based digital beam forming developed has great potential to be used for multifunctional phased array radar, launch vehicles traffic controller, climate monitoring and in providing wind velocity data for aircraft.

The new generation of radar has to be equipped with a high performance exciters and receivers to cope with the threat in an Electronic warfare scenario. The threat in a complex environment with interfering signals requires a reliable signal generation with proper frequency agility and efficient gain controls in receiver system. Such a system is designed by LGM Prakasam et al.[9](2007) – "Digital Signal Generator

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and Receiver design for S-band Radar". The design consists of exciter unit comprising of various digital modules for waveform generation, clocks and synchronization signal generation for different sub-systems of radar and digital code generation for the frequency to be synthesized. The utilization of the customized cores in the design models delivers high level of performance and area efficiency. Thus it resulted in an efficient implementation of the hardware using less percentage of FPGA resources. In addition, digital signals implementation proved to be advantageous because the system provided high flexibility, yet simple and reliable.

Digital multiple beam forming on every antenna element for a large phased array radar is not possible in processor based digital processing units, because it needs simultaneous processing of many A/D channels. As published in paper [10] (2014) – "A Digital multiple beam forming for phased array RADARs with parallel array processing", the authors have described methods to resolve this problem. The authors resolve the problem by using a multi array based beam forming technique with multiplexed signal processing unit on FPGA. The proposed mechanism employs multiplexed signal processing unit which is time shared for various beam formers. The technique ensures simultaneous beams without any compromise on functionality. In the proposed work the authors generated digital multiple beams with parallel array processing by using 16 antenna input signals. The design also provides a feasibility of implementing more than 16 antenna input signals.

TABLE II: BEAM FORMING SPECIFICATIONS.[10]

Parameter	value	comments
Input signal type	Band pass signal	Coming from typical superheterodyne receiver
Input signal frequency range	1.5-3.5MHz	2 MHz BWand 2.5MHz IF frequency value
Sampling rate	10MHz	
DDC filter size	16taps	
DDC decimation	4	DDC output sampling rate 2.5Msps
NCO values:COS	10.10	As $f_0 = f_s /4$
NCO value:SIN	0.101	As $f_0 = f_s /4$
Number of array elements	16	Linear array
Element spacing	3meters	

TABLE III: TRUE ANGLE VALUES OF BEAM [10]

DDS value	Angle
8	11.25
20	28.125
80	112.5
128	180

The proposed work by D.Subbarao et al.[11](2019) is more or less similar with the paper[5] mentioned above. The work "Multiple Digital Beamforming for Active Phased Array RADARs" implements methods to overcome the issue of processing A/D channels in digital multiple beam forming technology replacing antennas which hold large phased array radar by multiplexed signal processing unit. Working of each block in the system is explained briefly in the paper. The authors suggests the procedure of pillar shaping and the result of simulation and chip scope confirm maximum gain in desired direction and minimum in unwanted direction.

A wideband linear frequency modulated continuous waveform (LFMCW) radar echo signal simulator design scheme which is based on Agilent N8241A arbitrary waveform generators and E8267D vector signal generator is described by Jianchao Wang et al.[12] (2016) – "Study on Wideband LFMCW Radar Echo Signal Simulate Technique". The radar signal wave data is produced by computer and is changed to wideband IQ baseband signal by N8241A. Then, the baseband signal is inputted to Agilent E8267D, which switch the baseband signal to microwave radio signal by its IQ modulate function and output, for testing wideband LFMCW radar in lab. Experiment result indicate that the simulator possess not only wide using performance and high precision but also have simplified structure.

Wu Changrui et al.[13] (2010) – "Design and FPGA implementation of flexible and efficient digital down converters" has designed and implemented digital down converter(DDC) on Xilinx FPGA virtex-5. Compared with traditional ASIC DDC devices, DDCs implemented by FPGA have more flexible frequency and phase characteristics and higher precision computation. Having analysed the key points of DDC theory and MATLAB simulation analysis the authors have designed a DDC a clock cross region and first in first out (FIFO) interface characteristics using Xilinx ISE. The paper majorly discusses the theory of DDC and the details of implementation on Xilinx FPGA. The paper also includes an application describing an example of data flow in one DDC.

Yingying Du et al[14] (2016) – "Digital down conversion design and implementation based on FPGA". The authors of the paper have brought out a unique method of implementing FPGA based digital down conversion. Digital free mixing scheme is proposed by the authors to achieve digital down conversion on the basis of digital mixing orthogonal

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demodulation. This technique employed in the system will effectively reduce the computational complexity. The working principle is explained mainly including free mixing, design of cascade integrator comb filter and half band filter. FPGA implementation scheme is explained to prove the designed feasibility through software emulation.

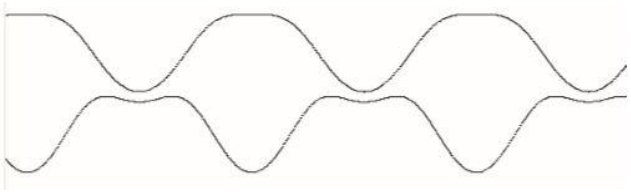

Figure 3: Simulation diagram after low pass filter.[14]

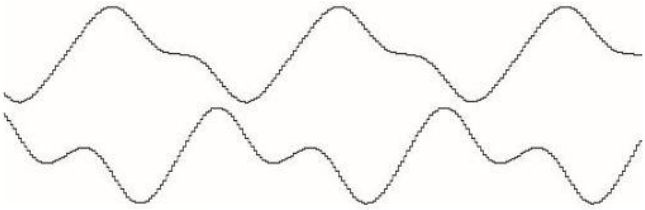

Figure 4: Simulation diagram after CIC filter.[14]

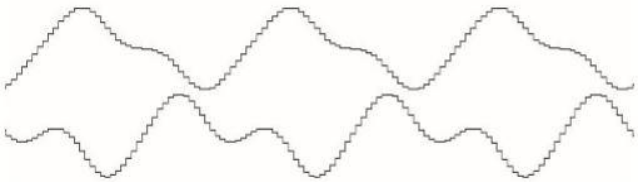

Figure 5: Simulation diagram after half band filter.[14]

TABLE IV: SUMMARY OF REVIEW OF LITERATURE

Authors	Title	Source	year	Findings
Shaya Karimkashi, Guifu Zhang, Redmond Kelley, John Meier, Robert Palmer, Allen Zahrai, Richard J. Doviak, and Dusan S. Zrnic	Cylindrical Polarimetric Phased Array Radar Demonstrator: Design and Analysis of a Frequency Scanning Antenna Array	IEEE	2013	Design, modelling and measurement results of a mid-size cylindrical polarimetric phased array radar.
Jeffrey S. Herd, David Conway M	The Evolution of Modern Phased Array Architectures	IEEE	2015	Using a tile array architecture, which greatly reduces the number of printed circuit boards and connectors in the array, substantial cost reductions are achieved
Long Pang, Bocheng Zhu, He Chen, Yizhuang Xie	A Highly Efficient Digital Down Converter in Wide Band Digital Radar Receiver	IEEE	2012	Increased requirements for miniaturization and low power consumption of signal processor in the digital wide band radar receiver.
Yogesh P Sajjan, Krishna R, Shahul H	FPGA Based Digital Beam Forming for Phased Array Radar	IJERGS	2015	Method to achieve digital beam forming in transmitter section. Implemented by designing a sixteenchannel direct – digital waveform synthesizer using Direct Digital Synthesizer
LGM Prakasam, Taniza Roy, Meena.D	Digital Signal Generator and Receiver design for S-band Radar	IEEE	2007	High performance exciters and receivers to cope with the threat in an Electronic Warfare scenario.
Nitesh Gaikwad, Radha Krishna AN	A Digital multiple beam forming for phased array RADARs with parallel array processing	IOSR-JVSP	2014	Inefficiency for simultaneously processing many A/D channels is resolved by using multi array based beam forming technique.
D.Subbarao, Tejavath Rama Krishna	Multiple Digital beam forming for Active Phased Array RADARs	IJRTE	2019	Multi arraybased beam forming technique with multiplexed signal processing unit on FPGA is implemented for active phased array radars
JianchaoWang, XiminLi, JianhuiWu	Study on Wideband LFMCW Radar Echo Signal Simulate Technique	IEEE	2016	A wideband LFMCW radar echo signal simulator design scheme which is based on Agilent N8241A arbitrary waveform generators and E8267D vector signal generator is designed.
Wu Changrui, Kong Chao, Xie Shigen, Cai Huizhi	Design and FPGA implementation of flexible and efficient digital down converters	IEEE	2010	The paper majorly discusses the theory of DDC and the details of implementation on Xilinx FPGA. The paper also includes an application describing an example of data flow in one DDC. Designed a DDC a clock cross region and first in first out (FIFO) interface characteristics using Xilinx ISE by analysing key points of DDC and Matlab simulation.
Yingying Du, Xinjing Ye, Yafei Li, Zhengyu Cai	Digital Down-Conversion Design and Implementation Based on FPGA	IEEE	2016	The authors of the paper have brought out a unique method of implementing FPGA based digital down conversion. Digital free mixing scheme is proposed by the authors to achieve digital down conversion on the basis of digital mixing orthogonal demodulation.

III. CONCLUSION

The study of literature provides information of FPGA based digital down converters. The proposed systems in different papers shows the step by step improvements in the waveform processing unit at the digital receiver and also describes the pulse compression, advantages of using FPGA based architecture. A detailed study on the above mentioned topic is carried out in this paper. The summary of the literature is described in table IV. This study leads to a conclusion that digital down conversion technique offers good digital stability.

IV. ACKNOWLEDGEMENT

The present work is an effort to study digital down conversion technique implemented on FPGA for phased array radars. The paper titled – "Study on Digital Down Conversion Technique Implemented on FPGA" would not have been possible to come to the present shape without the work done by all the authors mentioned in references. With deep sense of gratitude we acknowledge all the authors mentioned in the references and their work.

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