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Comparison of Power Estimation Between Reversible & Irreversible Logic Gates

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***Abstract*– In this article, basic irreversible gate (XOR gate) and basic reversible gates are designed using dataflow design. The output of all the basic gates are simulated and compared the power in Analyze power (Xpower) compiler. The combinational circuits (adder and subtractor) and sequential circuit (T flip flop) are designed using structural design with both conventional logic gates and reversible logic gates and power has been measured. Overall the power of conventional logic gates and reversible logic gates are compared that helps us to design gates with less power dissipation and more efficiency. All the individual reversible logic gates and complex combinational and sequential circuits are described in VHDL hardware description language and this circuits are functionally verified using Xilinx ISE 9.1i (student version) software.**

Keywords– **Reversible logic gates, power analysis, less power dissipation, VHDL**

I. INTRODUCTION

Gordon. E. Moore et al. (1965) predicted that the numbers of components on the chip will double every 18 months. Initially he predicted only for 10 years but due to growth in the integrated-circuit technology his prediction is valid till today [2]. His work is widely recognized as the Moore's law. The effect of Moore's law was studied carefully and researchers have concluded that as the number of components in the chip increases the power dissipation will also increase tremendously. It is also predicted that the amount of power dissipated will be equal to the heat dissipated by the rocket nozzle. Landauer et al. stated that the amount of energy dissipated to erase each bit of information is at least kTln2 (where k is the Boltzmann constant and T is the room temperature) during any computation the intermediate bits used to compute the final result are erased [1]. This erasure of bits is one of the main reasons for the power dissipation. C.H. Bennett (1973) revealed that the power dissipation in any device can be made zero or negligible if the computation is done using reversible model [10]. The most prominent application of reversible logic lies in quantum computers. It has applications in various research areas such as Low Power CMOS design, quantum computing, nanotechnology and DNA computing [7].

II. DESIGN OF BASIC LOGIC GATES

XOR gate- a logic irreversible gate and NOT gate (1*1), CNOT gate (2*2), Feynman Gate (2*2), Tofolli gate (3*3), Fredkin gate (3*3), Peres gate (3*3)- some reversible logic gates are designed using dataflow design of VHDL hardware description language and verified using Xilinx ISE 9.1i (SV) software [4-6].

Table 1. Truth table of XOR gate

Input		Output
A	**B**	**P**
0	**0**	**0**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

Fig. 1. Waveform of XOR gate

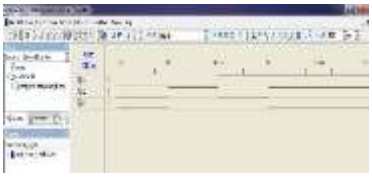

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Table 2. Truth table of NOT gate

X	Z= X'
0	1
1	0

Fig 2. Waveform of NOT gate

Table3. Truth table of CNOT gate

X	Y	X'	Y'
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Fig. 3. Waveform of CNOT gate

Table 4. Truth table of Feynman gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Fig. 4. Waveform of Feynman gate

Table 5. Truth table of Toffoli gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

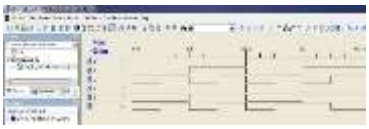

Fig. 5. Waveform of Toffoli gate

Table 6. Truth table of Fredkin fate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

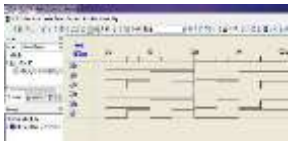

Fig. 6. Waveform of Fredkin gate

Table 7. Truth table of Peres gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

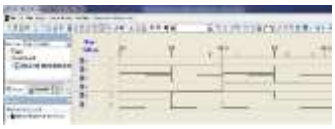

Fig. 7. Waveform of Peres gate

III. DESIGN OF COMBINATIONAL AND SEQUENTIAL CIRCUIT

A. COMBINATIONAL CIRCUITS-

Adder and subtractor are taken as example of combinational circuits. Combinational circuits consist of some basic logic gates. Full adder using irreversible logic gates consist of Half adder and OR gates, whereas reversible logic gates consist of Peres gates. In the other hand, Full subtractor using irreversible logic gates consist of Half subtractor and OR gate, whereas reversible logic gates consist of TR gates. This all gates are designed using structural design of VHDL hardware description language and verified using Xilinx ISE 9.1i (SV) software [8].

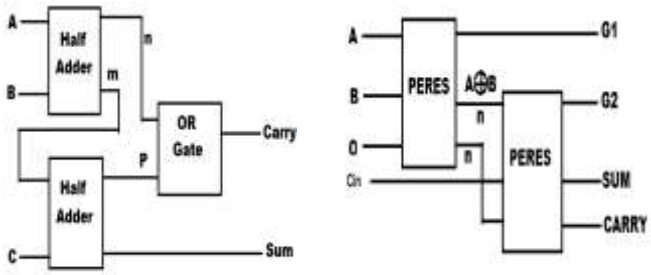

Fig. 8. Block diagram of Full adder using a. irreversible logic gates b. reversible logic gates

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Table 8. Truth table of Full adder

Input			output	
A	**B**	**C**	**Sum**	**Carry**
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**0**
0	**1**	**0**	**1**	**0**
0	**1**	**1**	**0**	**1**
1	**0**	**0**	**1**	**0**
1	**0**	**1**	**0**	**1**
1	**1**	**0**	**0**	**1**
1	**1**	**1**	**1**	**1**

Fig. 10. Waveform of Full adder a. irreversible logic gate b. reversible logic gate

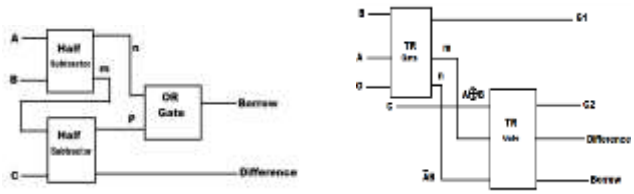

Fig. 11. Block diagram of Full subtractor a. irreversible logic gate b. reversible logic gate

Table 9. Truth table of Full subtractor

Input			output	
A	**B**	**C**	**Difference**	**Borrow**
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**1**
0	**1**	**0**	**1**	**1**
0	**1**	**1**	**0**	**1**
1	**0**	**0**	**1**	**0**
1	**0**	**1**	**0**	**0**
1	**1**	**0**	**0**	**0**
1	**1**	**1**	**1**	**1**

Fig. 12. Waveform of Full subtractor a. irreversible logic gate b. reversible logic gate

B. SEQUENTIAL CIRCUITS

Sequential circuits consist of some basic logic gates. Here T flip flop is taken as an example of sequential circuit. This T flip flop is made of two reversible logic gates SG gate and FG gate. This T flip flop is designed using structural design of VHDL hardware description language and the truth table is verified.

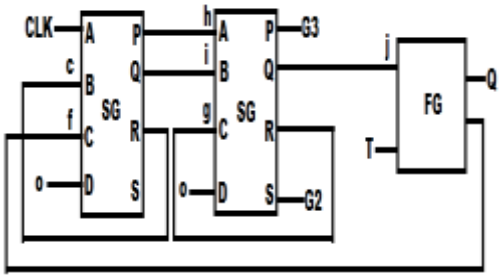

Fig. 13. Block diagram of T flip flop

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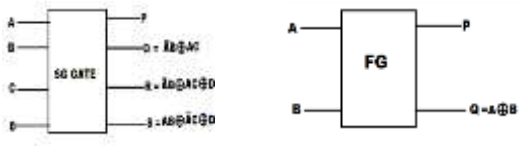

Fig. 14. Block diagram of SG and FG gates

Table 10. Truth table of T flip flop

Tn	Qn+1
0	Qn
1	Qn

IV. POWER ESTIMATION

Now, the power of all irreversible and reversible gates (basic gates, combinational circuits and sequential circuit) are compared in Analyze power (Xpower) compiler [8] and presented in the table below.

Table 11. Power calculation for Irreversible & Reversible Gates

Power Estimation		
Different Types of Gates	**Normal Logic**	**Reversible Logic**
Basic Gates	**23.50 mW**	**17.50 mW**
Combinational Circuits	**23.50 mW**	**17.50 mW**
Sequential Circuits	**25 mW**	**17.50 mW**

V. CONCLUSION

Matter of concern in this article is to reduce the power and to increase the efficiency. The goal is achieved by using reversible logic gates in basic gates, combinational circuits and sequential circuit. Here it can be seen that the power is increasing in complex circuits for normal logic, whereas the power is fix at a certain value for reversible logic gates. So, it can be used for complex circuits in quantum computing CMOS design nanotechnology etc.

In this article the power is analysed in Xilinx ISE 9.1i (SV) software[8] but if Cadence software[9] is used it will give more accurate results.

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