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SILICON INTERPOSER – A COST EFFECTIVE SOLUTION FOR PROTOTYPE PACKAGING OF MEMS ACCELEROMETER SENSORS AND ASSOCIATED ROIC

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***Abstract*— Assembly and packaging of accelerometer sensors and associated ROIC into a single compact package in an open tool Ceramic Pin Grid Array (CPGA) package with the help of a silicon interposer was explored as a cost effective solution. A Silicon Interposer was designed, fabricated and assembled in an open-tool 120 pin CPGA package**

Keywords— **MEMS sensors, accelerometer, ROIC, CPGA, Silicon Interposer**

I. INTRODUCTION

In a previous communication [1]**,** constraints associated with packaging of MEMS (Micro Electro Mechanical Sensors) accelerometers and associated Read Out Integrated Circuit (ROIC) into a single ceramic package were discussed in detail and a HTCC (High Temperature Co-fired Ceramic) solution was suggested to the customer. This approach involves substantial tooling costs that are justified only by large production volumes. Initially during prototype development a more cost effective solution, with minimum cost and turn around time, is required. Though the easiest way is to identify and use a commercially available suitable open-tool off the shelf package and then integrate the sensors and ASIC in a single package, problems and constraints involved in such an approach was discussed in detail and reported earlier [1,2]**.**

This paper describes an alternate and cost-effective solution in which a suitable Silicon Interposer may be designed and fabricated using the ASIC (Application Specific Integrated Circuit) and MEMS fabs available with the customer and then integration at package level may be carried out by selecting an appropriate off the shelf package. This paper reports design, fabrication and assembly of such a Silicon Interposer and its assembly in a 120 pin open-tool CPGA which enables integration of sensors as and when the same are fabricated.

Details of ROIC and Sensor chips proposed to be fabricated at Customer's MEMS fab were the same as described in a previous paper [1]**,** and as summarized in Table - 1.

Table - 1 Details of Customer chips and sensors

Sl.No.	Device	Form	Dimensions (mm)			Pad Orientations/ Remarks
			l	w	t	
1	ROIC ASIC	Die	4.5	4.5	0.7	40 (Top)+40 (Left)+ 12 (Bottom) **Note-1**
2	X,Y-Sensor	Die	2.1	3.8	0.7	**Note-2**
3	Z-Sensor	Capped Die	3.5	4.5	1.4	**Note-3**

Note-1: 14 pins on right side are to be bonded to XY-Sensor while 5 pins bottom side are to be connected to Z- sensor

Note-2: Total 14 pads on left side. None of the pads are connected to package pins. All the die pads are to be connected to respective die pads of ROIC

Note-3: Total 5 pads on bottom side and all the pads are to be connected to 5 corresponding bond pads on ROIC die (Bottom side)

II. SILICON INTERPOSER DESIGN

a) First step is to select a suitable open-tool ceramic package. Based on the dimensions and bond pad layout of sensors and ROIC, a 120 pin CPGA (Ceramic Pin Grid Array) package was selected.
b) Periferal pads of the Interposer are aligned with bonding pads of CPGA package while inner pads of the interposer are aligned with ROIC and Sensor die pads.
c)'Through cavities' in interposer are designed to accommodate the ROIC, XY and Z acceleration Sensors.
d) The layout takes care of design criterea such as minimum die spacing allowed, alignment of bonding pads among ROIC and sensor chips and package depth to facilitate comfortable wire bonding and hermetic sealing.

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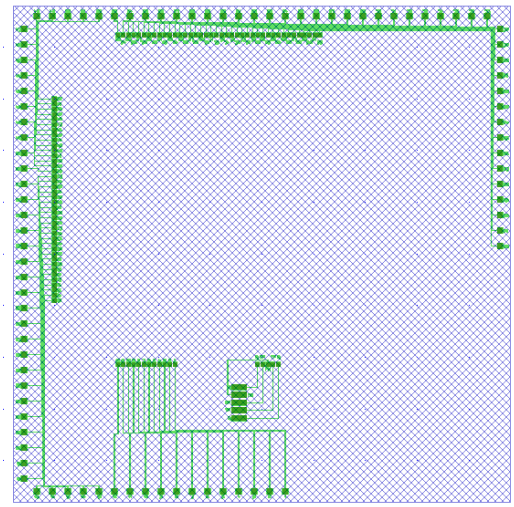

Fig. 1. Mask 1 for metal tracks and pads on interposer.

Fig.1 shows the pads and interconnecrions on the silicon interposer which is the Mask – I for lithography, while Fig.2 shows passivation mask, Mask-II, exposing only bonding pads.

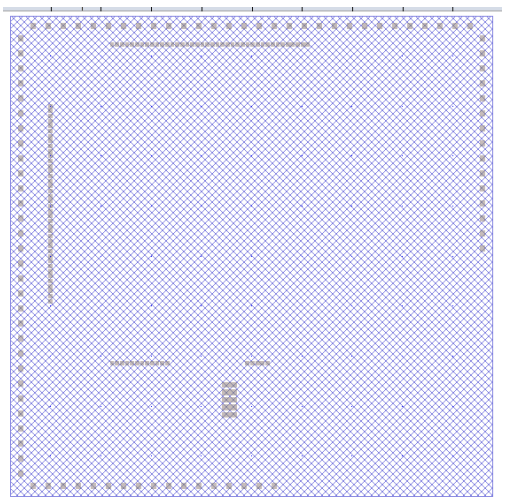

Fig.2. Mask 2 for passivation of interposer leaving out the bonding pads.

Fig.3 shows Mask-3, to realize through cavity in the interposer while Fig.4 shows the overall view with all the masks superimposed one over the other.

Fig.5 shows the tentative location of sensors within the cavity of interposer while Fig.6 shows the wafer map which describes positioning of dies on 6" wafer. As shown in the figure each wafer is designed to yield 36 interposers.

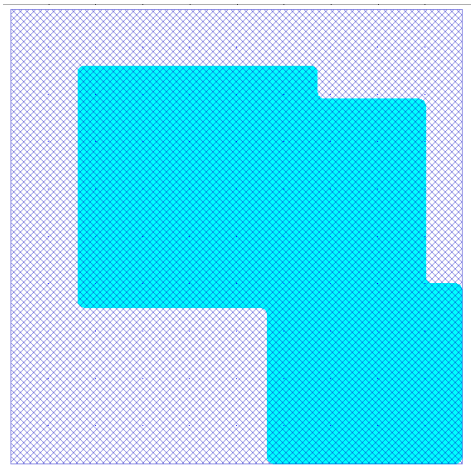

Fig. 3. Mask 3 for through cavity realization in the interposer.

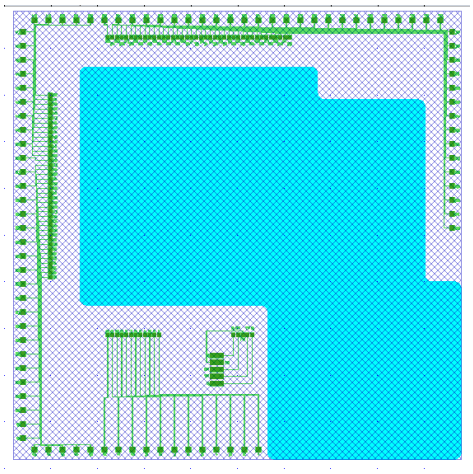

Fig. 4. Overall view with all the layers superimposed.

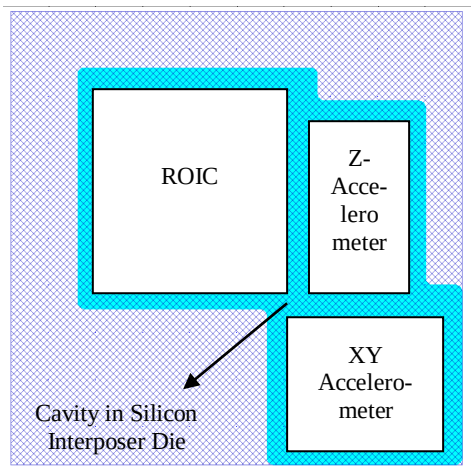

Fig. 5. Proposed positioning of sensos and ROIC.

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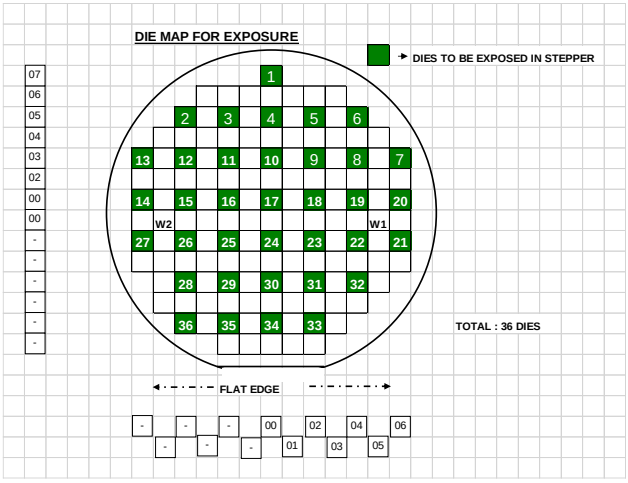

Fig. 6. Wafer Map

Alternate rows and columns are left blank for ease of handling while singulating the interposers.

III. SILICON INTERPOSER FABRICATION AND PACKAGING

Fig.7 shows the general process flow to realize the interposer. Starting material is a p-type bulk wafer 150mm dia and 675µm thickness. PM00 litho step and trench etch are to realize the alignment marks to be used for aligning subsequent layers. 1.0 µm Aluminium metallization is used for bonding pads and inter-connections. After 600µm bulk etching of silicon, the wafer is temporarily bonded to another bulk wafer with the help of an adhesive tape for subsequent handling.

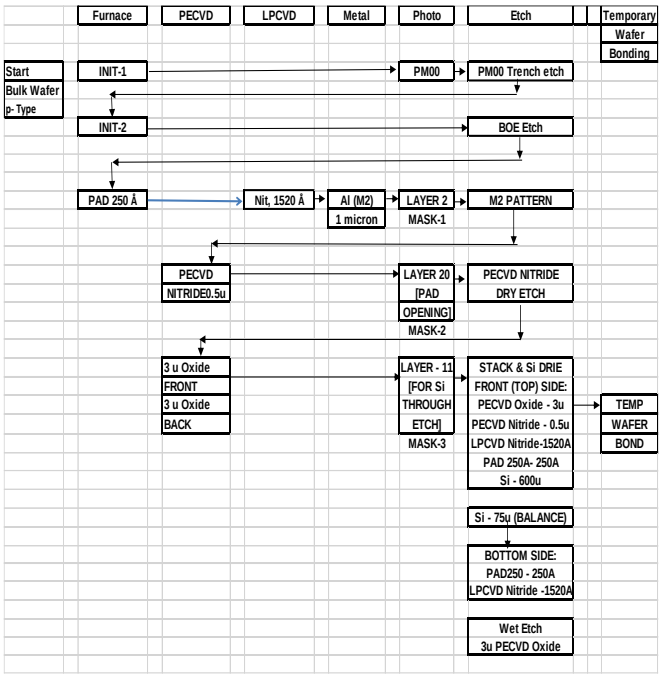

Fig. 7. Process Flow for fabrication of interposer.

Finally the wafer received was mounted on a dicing tape and diced into individual dies with the help of ADT 7200 Dicing machine. The interposer was subsequently bonded in an open tool 120 pin CPGA package. Interposer die attachment was done with epotek E4110 two part silver epoxy adhesive and epoxy was cured at 150° C for 15 minutes in oven in ambient.

Wire bonding was carried out with 18µm gold wire thermosonically with the help of F&K Delvotec Wire Bonder Model 5610.

IV. RESULTS AND DISCUSSIONS

Fig.8 shows details of assembled silicon interposer inside a 120pin CPGA without sensors. Space allotted for sensors is also shown in the figure.

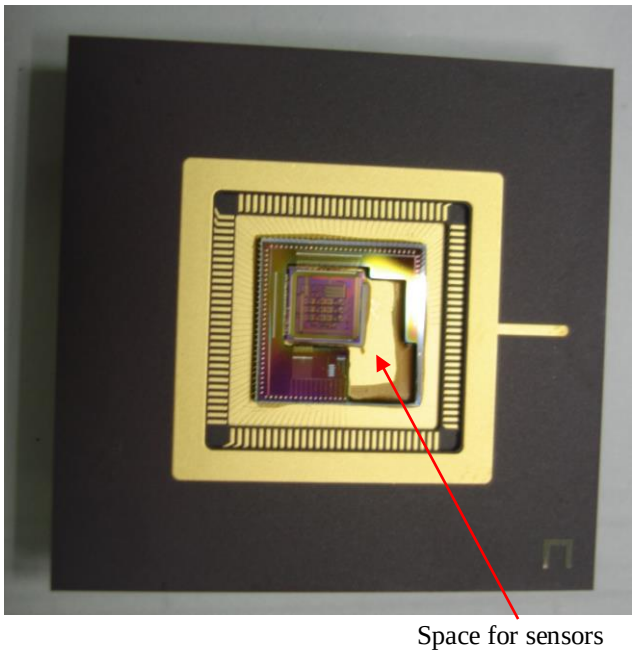

Fig. 8. Silicon Interposer assembled in 120 pin CPGA

Fig.9 and Fig.10 show the wire bonds between package pads – interposer pads and interposer pads-ROIC pads respectively.

Various problems such as wire sagging, complexity in configuring the wires from ROIC to package pads etc.. associated with, if ROIC and sensors were directly assembled in open-tool package, as discussed in earlier papers can be comfortably sorted out with the help of a silicon interposer. Unlike in HTCC approach, the silicon interposer can be easily realized in the same ASIC/MEMS fab thus reducing substantial tooling costs. This approach is very useful specially for prototyping, preliminary testing and evaluation.

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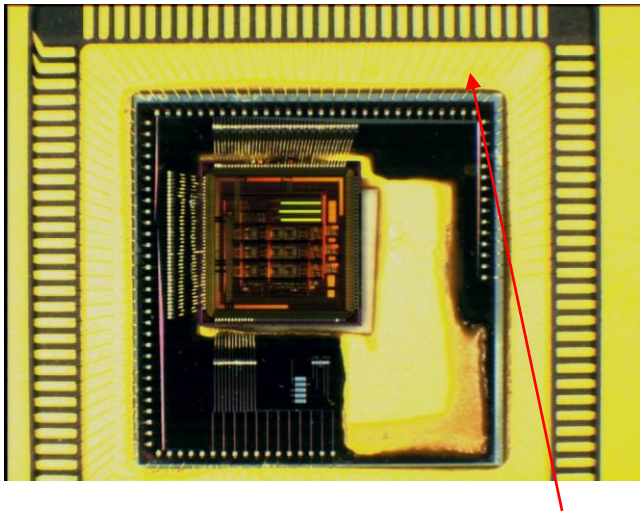
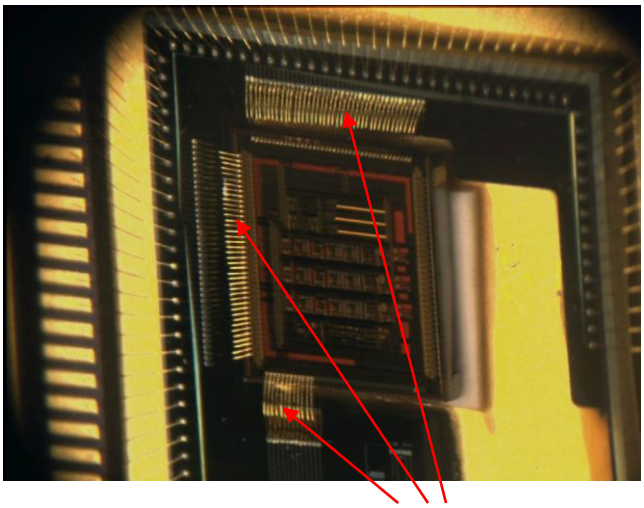


Wire bonds between interposer pads and Package pads

Fig. 9. Wire bonds between Silicon Interposer and Package pads



Wire bonds between ROIC die and Interposer pads

Fig. 10. Wire bonds between ROIC pads and Silicon Interposer pads

As and when sensor fabrication is completed the same may be easily assembled and integrated in the same package.

V. CONCLUSIONS

A cost effective solution for integrating MEMS sensors and ROIC with the help of a silicon interposer was explored. In the first stage the interposer with required cavity was designed, fabricated and assembled in a 120 pin CPGA successfully. As soon as fabrication of sensors is completed the same would be integrated in the same package.

VI. REFERENCE

1. K.S.R.C.Murthy, 'HTCC Approach for packaging MEMS Accelerometer Sensors and Associated ROIC', *Int.J.Adv.Res. (IJAR)* **6** (7), pp 537-552 (2018).

2. K.S.R.C.Murthy, 'Failure Analysis and Corrective Action in Wire Bonding of a Range Finder ASIC', *Int.Journ.Adv.Eng.Res and Science (IJAERS)*, **2** (9), Sep. 2015, pp 1 – 7 (2015).

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