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FPGA IMPLEMENTATION OF HIGH SPEED DCT COMPUTATION OF JPEG USING VEDIC MULTIPLIER

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***Abstract*— DCT is often used in image signal and processing based on lossy compression, it is one of the most effective techniques for image compression among various transform methods. DCT works by separating images into parts of different frequencies. This paper presents DCT computation of JPEG using Vedic Multiplier. In DCT computation steps matrix multiplication is one of the important step, DCT matrix is computed using Vedic multiplier. We have designed high speed 8*8 bit Vedic Multiplier in system generator. "Urdhva Tiryagbhyam" (Vertically and Crosswise) sutra is used to propose architecture of multiplication, which is quite different from conventional method of multiplication like add and shift. Use of Vedic multiplier in computation of DCT proposes low area, improved speed, energy efficient matrix multiplier.**

Keywords— **Compression, JPEG, DCT, Vedic multiplier, Urdhva Tiryagbhyam, FPGA**

I. INTRODUCTION

Computer technology provides flexible principles for processing large amounts of information. Among the algorithms available is **image data reduction**. The main principle of image compression is to reduce redundancy and irrelevance of image data. The principal approach in data compression is the reduction of the amount of image **data** (bits) while preserving **information** (image details).

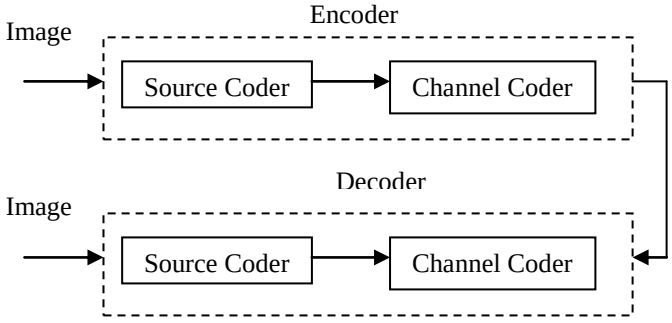

Figure 1. Generic Compression Scheme

Figure 1 shows basic image compression scheme, it consist of encoder and decoder.

Data compression techniques come in two forms: lossy and lossless.With **lossless compression**, every single bit of data that was originally in the file remains after the file is uncompressed. All of the information is completely restored. This is generally the technique of choice for text or spreadsheet files, where losing words or financial data could pose a problem. It can also be applied to image compression. The popular algorithms are the run length coding, Huffman coding, adaptive Huffman coding, arithmetic coding and dictionary based coding etc.

On the other hand, in **lossy data compression** original data is not exactly restored after decompression and accuracy of re-construction is traded with efficiency of compression.Generally a lossy technique means that data is saved approximately rather than exactly.Mainly used for image data compression and decompression. Compression ratio is high compare to lossless data compression technique. Lossy data compression algorithms are transform coding (for example, discrete cosine transform), Karhunen-Loeve Transform (KLT) and wavelet based coding(for example, continuous wavelet transform-CWT and Discrete wavelet transform(DWT).

DCT is one of the effective technique in Transform coding which has been used in image processing. N.Ahmed ,T.Natrajan and K.R.Rao described that DCT is one of the effective method which can be used in image processing. They have shown that the performance of DCT and other transform methods like Karhunen - Lo'eve transform are compare closely and optimal [1].

2D-DCT Design Architecture is used as core architecture for JPEG compressor.Lucian0 VolcanAgostini, Ivan Saraiva Silva and Sergio Bampi described simplified algorithm to compute 2D-DCT, here image data is divided into 8 by 8 block of pixels and DCT is applied to each block [5].

Multiplication is one of important arithmetic operation in DCT computation. Speed is one of the constraints in such operation and here use of Vedic multiplier increase the speed and hence results in increased performance of the System [10] [11].

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S. S. Kerur1, Prakash Narchi2, Harish M Kittur3, Girish V. A4. Implemented DCT algorithm using Vedic multiplier. They have used matrix multiplication method for DCT computation and Vedic multiplier which is designed using VHDL is used to compute the multiplications which consumes less time [9].

Vedic multiplier is designed using Ancient Vedic Mathematics technique. Vedic mathematics is based on sixteen sutra. As per research done by Ms.S.V.Mogre, Mr.D.G.Bhalke, UrdhvaTriyagbhyam sutra is generally used for multiplication of decimal numbers which is literally means vertical and cross- wise. Due to less no. of computation steps in Vedic multiplier results in increased speed, high performance and low power consumption [10].
Transform encoding is the type of encoding used for JPEG images for image compression. The DCT is transform method which is often used in JPEG image compression. DCTs are important to numerous applications in science and engineering, from lossy compression of images.

DCT

Discrete Cosine Transform is one of the key components of JPEG image compression. This is the process of separation of input image data into different frequency components. DCT is more similar to the DFT where decomposition of input signal into harmonic cosine function is done. Use of DCT in image compression results in energy compaction, bit savings which is our key requirement in image processing.
We have used below formula for the computation of DCT. Below equation computes (i , j) entry of the DCT of input image.

$$D(i,j) = \left(\frac{1}{\sqrt{N}}\right) C(i)C(j) \sum_{x=0}^{N-1}\sum_{y=0}^{N-1} p(x,y)\cos\left[\frac{(2x+1)i\pi}{2N}\right]\cos\left[\frac{(2y+1)j\pi}{2N}\right]$$

Where,
N is block size i.e. here we considering block size N=8.
C(i,j) is the intensity of the pixel in row i and column j.
D(I,j) is the coefficient of the DCT matrix.
P(x,y) intensity value of pixel.

Vedic Multiplier Design
There is a wide range of multiplication techniques among them classic long multiplication algorithm is most familiar to the majority of people. The designed multiplier is based on Vedic Multiplication Techniques; these are used for multiplication of two decimal numbers. In this multiplier we have applied same techniques of Vedic multiplication for multiplying binary numbers which is compatible with the digital hardware system. Multiplier design is based on Urdhava Tiryakbhyam sutra explained as below:

Urdhava Tiryakbhyam(Vertically and Crosswise)

The proposed multiplier design is based on Urdhava Tiryakbhyam Sutra (Vertically and Crosswise) of Ancient Indian Vedic Mathematics Techniques.Urdhava Tiryakbhyam is general Sutra/Method that can be used for multiplication of any two numbers. It means vertically and crosswise.
The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel. As the multiplications are performed independent of the clock frequency of the processor. The processing power of multiplier can easily be increased by increasing the input and output data bus widths because of its regular structure. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly.
Multiplication of two decimal Numbers: To illustrate vertical and crosswise multiplication let us consider multiplication of two decimal numbers 252 * 486,

Step 1		Step 2	
2 5 2	Result=12	2 5 2	Result=46
4 8 6	Pre Carry = 0	4 8 6	Pre Carry= 1
2	12	7 2	47

Step 3		Step 4	
2 5 2	Result=60	2 5 2	Result=36
4 8 6	Pre Carry = 4	4 8 6	Pre Carry= 6
4 7 2	64	2 4 7 2	42

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Step 5

2 5 2
| Result=8
4 8 6 Pre Carry = 4

1 2 2 4 7 2 12

Vedic Multiplier for 2x2 bit Module

The method is explained below for two, 2 bit numbers A and B where A = a1a0 and B = b1b0 as shown in Fig. 4. Firstly, the least significant bits are multiplied which gives the least significant bit of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit of the final product

$$s0 = a0b0 \quad (1)$$
$$c1s1 = a1b0 + a0b0 \quad (2)$$
$$c2s2 = c1 + a1b1 \quad (3)$$

The final result will be $c2s2s1s0$. This multiplication method is applicable for all the cases.

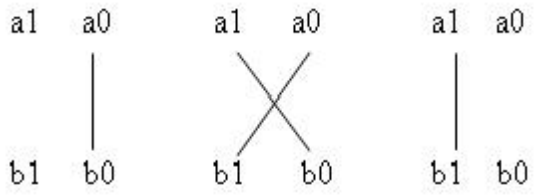

Fig.2 The Vedic Multiplication Method For Two 2 Bit Binary Numbers

Fig (a) shows the Vedic multiplier design which we have designed using System Generator.

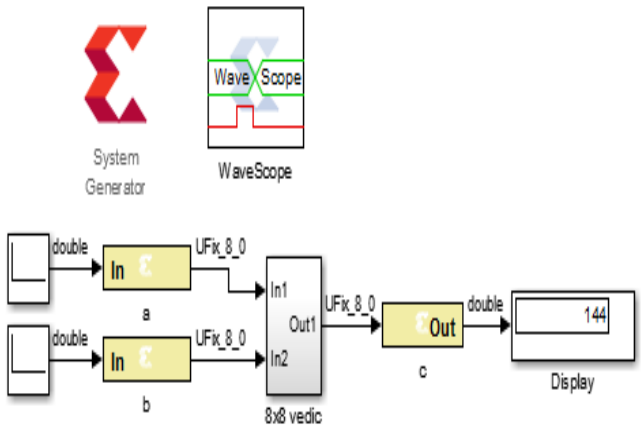

Fig 3: Fig. MATLAB Implementation of 8x8 Vedic Multiplier

II. Proposed Algorithm

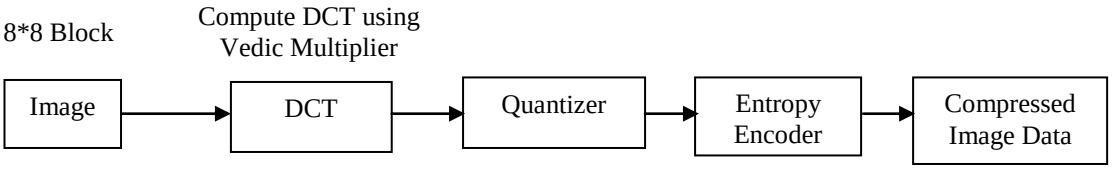

Fig. 4. 1DCT Based Encoder

Below algorithm illustrates the general process of image compression:

1. Take any Size of input image; here we have taken grey scale image.
2. Divide image into 8 by 8 blocks.
3. Working from left to right and top to bottom DCT is applied to each block.
4. Each block then compressed using quantization.
5. The array obtained from the quantization of each block have reduced amount of data.

Compressed image is reconstructed using decompression

III. Result Analysis

Basically image compression of the input data by using Vedic multiplier is implemented using System generator. And results of the System generator image compression is compared with Matlab image compression results. System generator 14.2 is used for the synthesis of the design. Figure 5 shows system generator design. DCT is implemented using system generator and all the multipliers are replaced with Vedic multiplier shown in section II.

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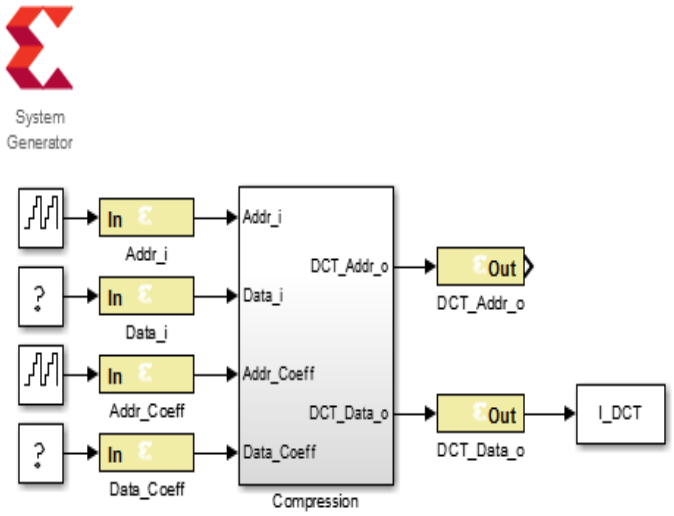

Fig. 5. System Generator Design

We have taken input image data using Matlab and DCT computation is synthesized in system generator and further quantization is done in Matlab. In the given design insert compression Factor between 1-100% as shown in below screen Figure (1).

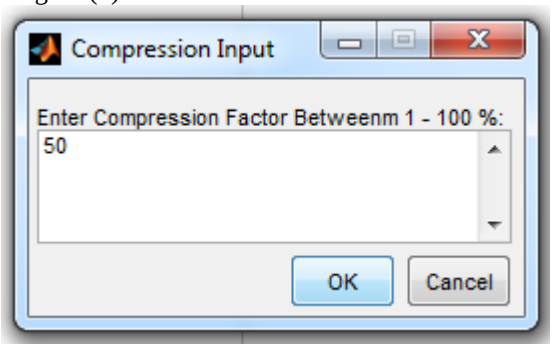

Fig. 6: Input Compression Factor

Figure (2): Shows the input image for image compression and fig (3) shows the compressed image with compression factor 20% with PSNR.

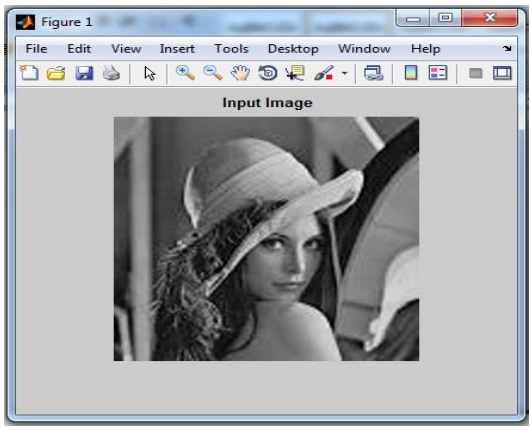

Fig. 7.Input Image

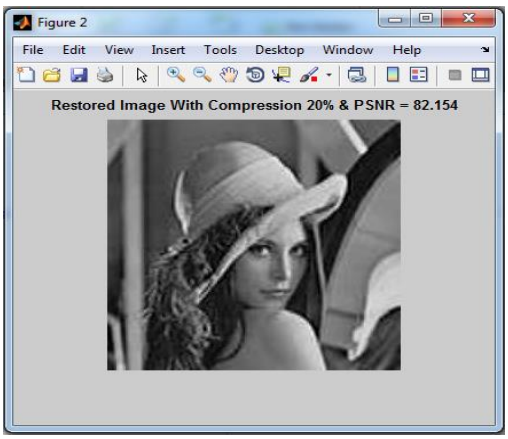

Fig. 8. Compressed Image

Fig (8) shows results of Vedic multiplier which we have designed in System generator explained in section (II)

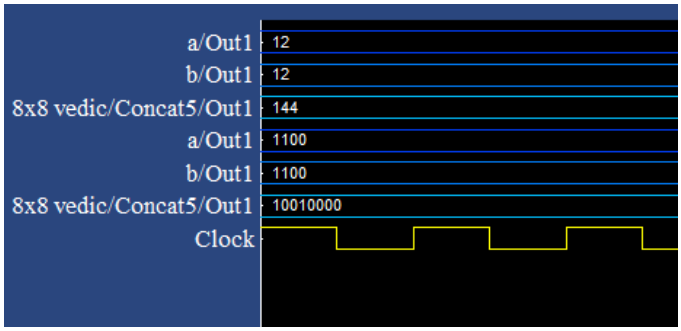

Fig. 9. Wave scope Window

IV. Conclusion

This paper presents an effective architecture design for DCT computation based on the Vedic Mathematics on FPGA's for grey scale images. Standard test images are used to test functionality of design. Result shows increased speed of processing by the use of Vedic multiplier (Urdhava Tiryakbhyam). Proposed architecture is area and power efficient compared with other architectures, with high accuracy in terms of PSNR.

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