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# DESIGNING OF DIFFERENT TYPES OF OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Manoj Kumar Dahiya
Student, ECE. (P.T.)
Hisar, India

Deepak Sharma
Assistant Professor, ECE, OITM
Hisar, India

***Abstract*— The operational transconductance amplifier (OTA) is one of the most important basic blocks used in the design of analog integrated circuits (ICs). However, its optimization involves a large number of parameters and specifications that have to be accurately adjusted during the simulation process to appropriately achieve the design goals. This work addresses the whole framework required to the automatic design of an OTA, from its architecture to manufacturing. In this Paper we represent designing of different types of OTA amplifier along with their advantages and disadvantages by use of various techniques.**

**Keywords—Transconductance, Cascode, OTA, Transistor, Channel**

## I. INTRODUCTION

For High speed high accuracy circuit, op-amp with high open loop Dc gain for the settling accuracy of 1% less than 30ns high output swing due to large output dynamic range specification of 85 db high unity gain bandwidth are required. This indicates that the chosen topology must have large output swing as well as minimal noise. Our target is to design an amplifier with 300MHz unity gain bandwidth and a dc gain higher than 80db .This OTA is intended to work in a switched capacitor integrator in the first stage of a delta sigma modulator[16] .The first, and probably the most important step of the design is to select an amplifier topology that possess the ability to meet all the specification using the least amount of power .Due to the high close loop gain and the extremely small allowable settling error of 0.01% a quick calculation reveals that the amplifier must be able to deliver an open loop gain of 80db .Gain boosting is very attractive because booster can multiply up the gain of the main amplifier while consuming minimal power an important concern when utilizing gain booster is the pole zero doublet, which must be placed at a high enough frequent to prevent it from slowing the settling but not so high that it causes [17] significant ringing around the local gain booster loop.

Topology that will certainly satisfy this magnitude of DC gain include a two stage amplifier with either a telescope or folded cascade first stage a gain booster amplifier or a folded triple cascade. To avoid much complexity in the design process a two stage topology is chosen .The 85db dynamic range specification calls for a careful comparison between single stage and two stage topology .In a two stage implementation, the second stage can be design to provide a larger output swing of 3v thereby reducing the capacitance driven by the input transistor and consequently lowering the required current in the first stage .However the second stage generally needs to flow at least the same amount current as the first stage to allow for slewing during amplifier operation .The OTA current required for the two stage topology would therefore be at least double that of the first stage. Hence, if a single stage amplifier can achieve output swing higher than 2.3V, it would dissipate lower power than a two stage amplifier. In term of circuit topology, telescopic is the necessary choice over folded cascade in order to realize this benefit to decreased power since a telescopic amplifier consume only half as much power and produce less noise at the expense of a slightly tighter output swing [18].

### *A. Telescopic cascode op-amp*

Telescopic cascode op-amp as shown in figure 1.1 typically has higher frequency capability and consume less power and then other topology. Its higher frequency response stem from the fact that its second pole corresponding to the source node of the n-channel cascode device is determined by the transconductance of n- channel device as opposed as p-channel device, as in the folded cascode .Also the parasitic capacitance at this node arises from only two transistor instead of three, as in the latter. The single stage architecture naturally suggests low power consumption. Historically, VLSI designers have used circuit speed *85* the "performance" metric. Large positive in terms of performance and silicon area, have been made for digital processor, microprocessors, DSPs (Digital Signal Processors) etc. In general, "small area" and "high performance" are two crediting constraints. The IC

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designers' activities have been involved in trading off this constraint. Power dissipation issue was not sign criterion but an afterthought. In fact, power considerations have been the ultimate design criteria in special portable applications such as wristwatches and pacemakers for a long time and the objective in these applications war minimum power for maximum battery life time.

Recently, power dissipation is becoming an important constraint in *B* design. Several reasons underlie the emerging of this issue. Among them we date Battery-powered systems such *BS* baton/notebook campouts, electronic organizer, etc. We need for these systems arks from the need to extend battery we. Many portable electronics use the rechargeable Nickel Cadmium (NiCad) batteries. Although the battery industry has been making efforts to develop batteries with higher energy capacity than that of NiCad, strident increase does not seem imminent. The expected improvement of the energy density is 40% by the turn of the century. With incent NiCad batteries, the energy density is around 20 Watt W hour/pounds and the voltage is around 1.2 V. So, for example, for a notebook consuming a typical power of 10 Watts and using 1.5 pound of batteries, the time of operation bidden recharges is 3 hours. Even with the advanced battery 2V.

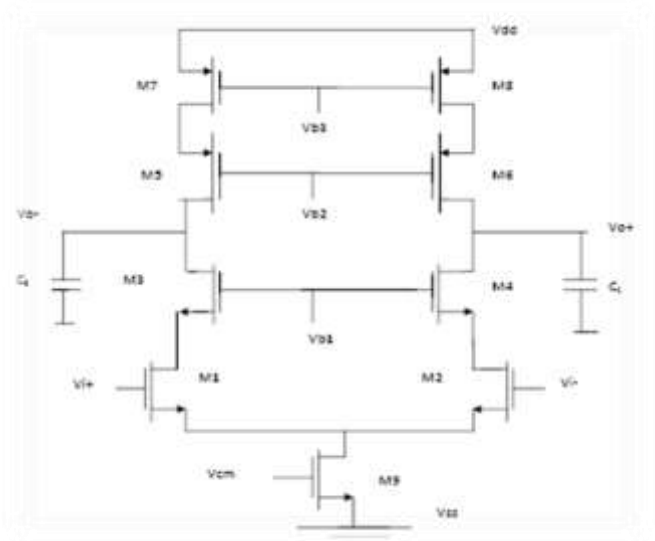


Figure 1.1: Telescopic differential amplifier

## II. Design of Two Stages Telescopic Fully Differential OTA

The differential amplifier is the basic building block of operational amplifier, the discussion of differential amplifier in this section sets the groundwork for analysis and design procedures for the operational amplifier. The analysis of differential amplifier not only classifies the operation of the operational amplifier but also makes the characteristic of the operational amplifier easy to understand. In addition, the analysis procedure developed in this section provides a means of checking operational amplifier parameters such as voltage gain and input and output resistance that are specified on the manufacturer's data sheets. Differential Amplifier is the ultimate amplifier. It is a special type of amplifier, which can amplify the difference of input signals. Hence, it is called differential amplifier [19]. It is used in another special type of amplifier circuit called Operational Amplifier (OPAMP). The differential amplifier has two inputs: inverting input (input –1) and non sin inverting input (input –2). Its output signal is 180° out of phase with inverting input signal and in phase with non-inverting input signal. For example, when negative voltage is connected to inverting terminal we get positive voltage at output. Similarly, when negative voltage is connected to non-inverting terminal, we get negative voltage at output. The figure shows circuit of differential amplifier. It is symmetrical circuit, i.e. it has same components on both sides. It works in two different modes: the differential mode and the common mode, as in this section we discuss various step to follows in the designing of the fully differential with having target specification.

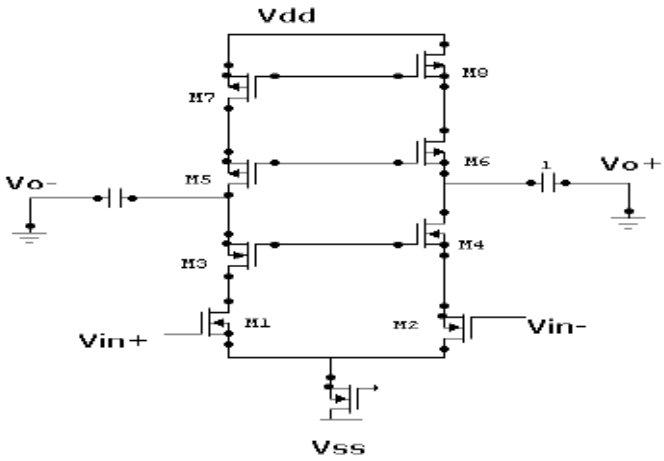


Figure 2.1: Simple telescopic amplifier

The first step of any two stage design is the design of input differential stage amplifier which is telescopic differential in our case .The input transistor of the of the telescopic cascode stage are NMOS device to maximize gm/id. For the second output stage, a common source amplifier for each differential output was utilized as typically done. Differential amplifier as output stage would be more complicated due to the design of another common feedback circuit. In addition the tail current transistor for the differential amplifier will only consume voltage head room thus lowering the output swing .To ensure stability of the amplifier ,miller compensation is used despite the cascode compensation better high frequency performance. Miller compensation however, can be easily designed and will introduce non –negligible noise depending on how the circuit is compensated.

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## III. DIFFERENT CONFIGURATION OF OTA

There are different configurations of OTA topologies. Each topology has its own advantage and disadvantage.

### i. Single –Stage OTA

Single stage OTA is as shown in figure 3.1. This single stage OTA is less complex compare to other types of OTA topology. Because of its less complex property its speed is higher compare to other topology. The drawback of this type of OTA is lower gain due to the fact that output impedance of this type configuration is relatively low. However this low impedance also leads to high unity gain bandwidth and high speeds. The Operational Tran conductance Amplifier (OTA) is the block with the highest power consumption in analog integrated circuits in many applications. Low power consumption is becoming more important in handset devices, so it is a challenge to design a low power OTA. There is a trade-off between speed, power, and gain for an OTA design because usually these parameters are contradicting parameters. There are three kinds of OTAs: two stage OTAs, folded-cascode OTAs, and telescopic OTAs. The telescopic amplifier consumes the least power compared with the other two amplifiers, so it is widely used in low power consumption applications. It has also high speed compare to other two topologies [20-21]. An operational Tran conductance amplifier (OTA) is a voltage input, current output amplifier. The input voltage $V_{in}$ and the output current $I_{out}$ are related to each other by a constant of proportionality and the constant of proportionality is the transconductance gm of the amplifier

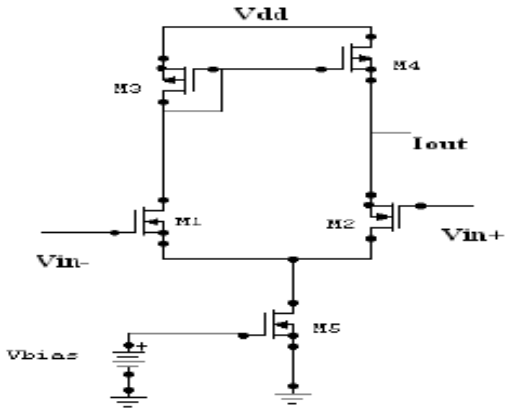


Figure 3.1: Single stage OTA

### ii. Two –Stage OTA

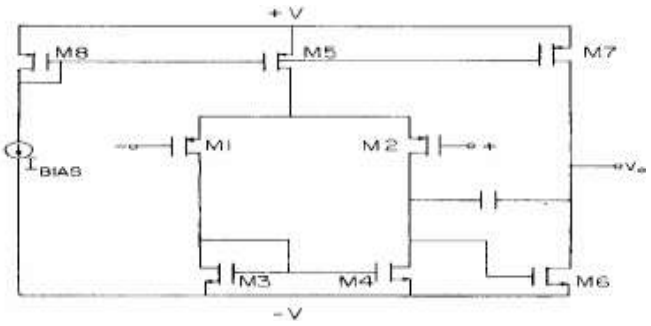


Figure 3.2: Two Stages OTA

as shown in figure. 3.2. That is basic circuit diagram of two stages OTA. In which M1and M2 use for differential input pair, M3 and M4 forms current the setup for deriving the bias conditions is as follows. The input terminals are the same DC potential, the common-mode input voltage Vcm. We assume that the common-mode input voltage is allowed to range between a minimum value Vcm; min and maximum value Vcm: max, which are given. Similarly, we assume that the output voltage is allowed to swing between a minimum value Vout; min and a maximum value Vout; max (which takes into account large signal swings in the output).The bias conditions are that each .transistor M1….M8 should remain in saturation for all possible values of the input common-mode voltage and the output voltage.

- Transistor M1: The lowest common-mode input voltage, Vcm; min imposes the toughest constraint on transistor M1 remaining in saturation.
- Transistor M2: The systematic offset condition makes the drain voltage of M1 equal to the drain voltage of M2. Therefore, the condition for M2 being saturated is the same as the condition for M1 being saturated. Note that the minimum allowable value Vcm; min is determined by M1 and M2 entering the linear region.
- Transistor M3: Since Vgd3=0 transistor M3 is always in saturation and no additional constraint is necessary.
- Transistor M4: The systematic offset condition also implies that the drain voltage of M4 is equal to the drain voltage of M3. Thus M4 will be saturated as well.
- Transistor M5: The highest common-mode input voltage, Vcm; max, imposes the tightest constraint on transistor M5 being in saturation the maximum allowable value of Vcm; max is determined by M5 entering the linear region.
- Transistor M6: The most stringent condition occurs when the output voltage is at its minimum value Vout; min.

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- Transistor M7: For M7, the most stringent condition occurs when the output voltage is at its maximum value Vout; max.
- Transistor M8: Since Vgd8=0, transistor M8 is always in saturation; no additional constraint is necessary.M9, M10, M11, M12 forms cascade current biasing circuit. In summary, the requirement that all transistors remain in saturation for all values of common-mode input voltage between Vcm;max and Vcm;max, and all values of output voltage between Vout; min and

$V_{out}$; max. We start by considering some very basic constraints involving the device dimensions, e.g., symmetry, minimum or maximum dimensions, and area limits.

*A. Symmetry and matching*

W1=W2, L1=L2, W3=W4, L3=L4 (3.1)

The biasing transistor M5 and M8 must match, i.e. have same length:

L5=L8 (3.2)

The five equality constraints in 3.1 and 3.2 have monomial expressions on the left and right hand side.

*B.* Systematic input offset voltage

To reduce offset voltage, the drain voltages of M3 and M4 must be equal, ensuring that the current from M5 is split equally between transistor M1 and M2 [22]. This happen the current densities of M3, M4 and M6 are equal. These two conditions are equality constraints between monomials, and are therefore readily handled by geometric programming *C.* Bias conditions, signal swing, and power.

*C.* Constraints

In this section we consider constraints involving bias conditions, including the effects of common-mode input voltage and output signal swing. We also consider the quiescent power of the op-amp (which is determined by the bias conditions). In deriving these constraints, we assume that the symmetry and matching conditions (1) and (2) hold. To derive the equations we use a standard long channel, square-law model for the MOS transistors, which is described in detail. In order to simplify the equations, it is convenient to define the bias currents I1, I5 and I7 through transistors M1, M5 and M7 respectively. Transistors M5 and M7 form a current mirror with transistor M8. Their currents are given by:

$$I_5 = \left(\frac{W_5 L_8}{L_5 W_8}\right) Ibias \quad , \qquad (3.3)$$

$$I_7 = \left(\frac{W_7 L_8}{L_7 W_8}\right) \qquad (3.4)$$

Thus I5 and I7 are monomials in the design variables. The current through transistor M5 is split equally between transistor M1 and M2.Thus we have:

$$I_1 = \frac{I_5}{2} = \left(\frac{W_5 L_8}{2 L_5 W_8}\right) Ibias \qquad (3.5)$$

Since these bias currents are monomials, we can include lower or upper bounds on them or even equality constraints, if we wish. We will use I1, I5 and I7 in order to express other constraints, remembering that this bias current can simply be eliminated.

*D.* Gate overdrive

It is sometimes desirable to operate the transistors with a minimum gate overdrive voltage. This ensures that they operate away from the sub threshold region, and also improves matching between transistors.

*E.* Quiescent power

The quiescent power of the op-amp is given by:

$$P = (V_{dd})(I_{bias} + 15 + 17) \qquad (3.6)$$

Table 1 shows that the aspect ratios of all transistor to operate in saturation.

Table 1 TRANSISTOR ASPECT RATIOS:

| **Transistor** | **W/L ratios** |
|---|---|
| M1,M2 | 10/0.35 |
| M3,M4,M5 | 1.4/0.35 |
| M6 | 34/0.35 |
| M7 | 12/0.35 |
| M8,M9,M10,M11,M12,M13 | 1.4/0.35 |

The second stage gain stage is simply a common source gain stage with the p-channel active load. Here pole-zero compassion is used. Bias circuit is actively designed.

**Advantage**

1. It has high output voltage swing.
2. It has higher gain compare to single stage OTA.

**Disadvantage**

1. It has a compromised frequency response.
2. This topology has high power consumption because of two Stages in its design.
3. It has a poor negative Power Supply Rejection at higher Frequencies.

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## IV. TELESCOPIC CASCODE OTA

In this design telescopic OTA is used because of its simplicity over other designs, allowing for higher-speed operation. In a folded-cascode design, there is an input differential pair and two separate current branches for the differential output. The input currents are mirrored with a cascode configuration to produce the output currents. The telescopic architecture puts both the input differential pair and the output on the same two current branches. This approach eliminates the noise problems caused by the current mirrors and also leads to a more direct signal path, which allows for higher speed. Another advantage of the telescopic architecture is that it uses half the bias current of a folded-cascode design because it has two fewer branches for current [23].The Telescopic Cascode OTA configuration is as shown in figure 4.1.

**Advantage**

1) It provides higher speed.

2) It has lower power consumption.

**Disadvantage**

1) Limited output swing.

2) Shorting the input and output is difficult.

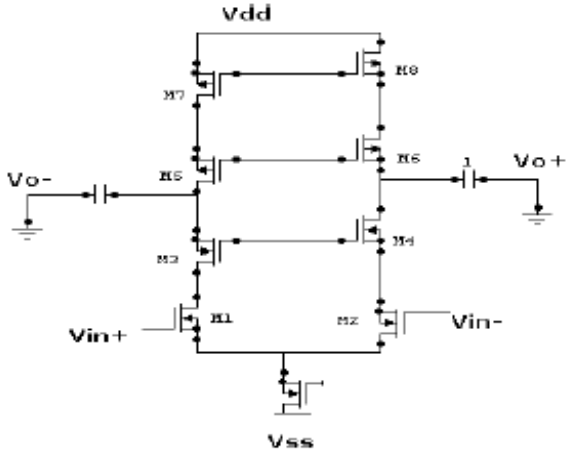


Figure 4.1: Telescopic Amplifier

## V. FOLDED CASCODE OTA

The structure of the folded cascade OTA is indicated In Fig.5.1. By using the cascade stage and common-drain stage, the driving ability is better than before and the bandwidth has been broadened while the dominant will not be influenced.

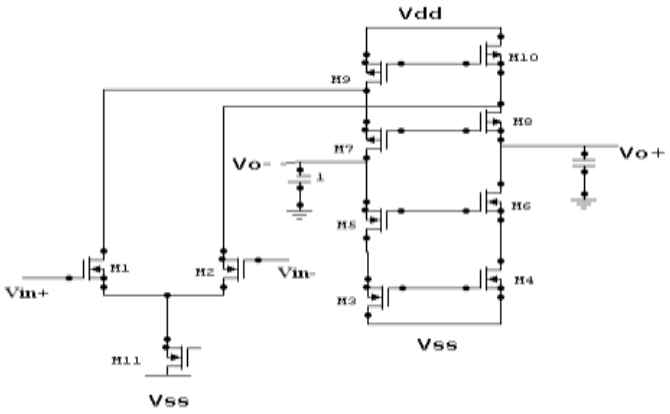


Figure 5.1: Folded cascode OTA

**Advantage**

*1)* This design has corresponding superior frequency response than two – stage operational Amplifiers.

*2)* It has better high frequency Power Supply Rejection Ratio.

**Disadvantage**

1) Folded cascode has two extra current legs, and thus for a given settling requirement, they will double the power dissipation.

2) The folded cascode stage also has more devices, which contribute significant input Referred thermal noise to the signal.

## VI. FUTURE SCOPE FOR WORK

In Future there are many possibilities of research on this topic. This section summarizes a few potential future directions for this work.

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