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HALF ADDER DESIGN USING VARIOUS TECHNOLOGIES AND COMPARISON OF VARIOUS PARAMETER PERFORMANCE

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Abstract: In this paper, investigate and analysis various techniques for implementing a half adder circuit with the fewest transistors possible. In digital electronics half adder combinational circuit used to add two numbers. It is an arithmetic circuit that performs the arithmetic operation of adding two single-bit words. The half adder technique, design of half adder using AVL technology, Design of a 3-T Half Adder, NMOS pass transistors logic design of half adder using 2:1 MUX, half adder circuit design with CMOS NAND gates, half adder circuit design with CMOS transmission logic gates in cadence virtuoso. In this section, compare half adder circuit design techniques and compare various parameters of half adder circuit design used various circuit design techniques. Conventional techniques required fewer number routing resources. A 3-T half-adder circuit performs with less delay, high speed, small layout area, less power consumption and batter efficiency and accuracy.

Keywords: Half adder, CMOS technology, AVL technology, MUX and pass transistor, Conventional design.

I. INTRODUCTION

In digital electronics: Combinational design are time-independent and only relies on present inputs. Combinational design is incapable of storing any state. Combinational design is simple to design, have a high speed, are time-independent, and can be used for ALU and Boolean operations. The combinational logic circuits do not have a clock and do not need to be triggered. The combinational design does not have a memory element.

Design techniques: On cadence virtuoso, a half adder implemented using universal gates, pass gates transistors with 2:1 mux and transmission gates.

A and B are two single binary digits used for half adder circuit. It gives two output : carry(c) and sum(s). For more than two-digit addition, they carry signal represents an overflow into the next digit and sum(s) is equal to 2C+S. Most basic half adder circuit design using XOR and AND logic gates, XOR gives the sum(s) and AND gives the carry(c). The Boolean logic will be A'B+AB', and for the carry, AB.

Fig.1 Block diagram for half adder

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table.1 Truth table for half adder

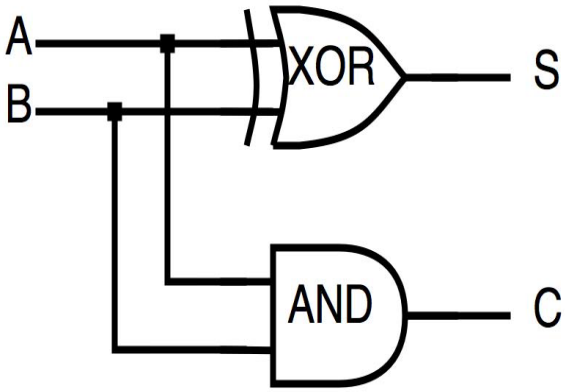

Fig.2 Half adder circuit diagram

II. PROPOSED ALGORITHM

A. HALF ADDER CIRCUIT DESIGN USING CMOS NAND GATES ON CADENCE VIRTUOSO

Design CMOS technology to design the NAND gate, it's consists of two parallel PMOS transistors connected with the two NMOS transistors in series, after on cadence

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virtuoso we implement the half adder circuit design with NAND universal gates.

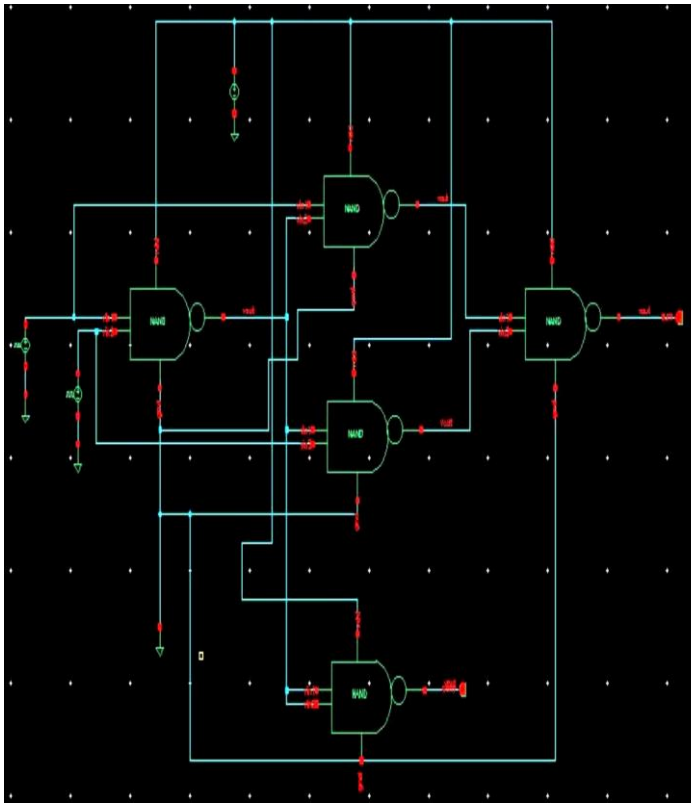

Fig.3 Half adder circuit design using CMOS NAND gates on cadence virtuoso [1].

NAND gates were used to create a half adder. To design, any type of digital circuit used a universal gate. Here NAND gate used to design for half adder circuit because NAND gate is a universal gate. It is always simple and efficient to use the fewest number of gates possible when designing our circuit. A half adder requires a minimum of 5 NAND gates to be designed.

NAND gate accepts two 1-bit numbers as inputs. The resulting NAND-operated inputs, along with the original input, will be fed back into three NAND gates. Out of these three NAND gates, two will generate output, which will be fed into the NAND gate at the other end. The sum bit will be generated by the gate connected at the end. The carry bit will be generated by the third of the three NAND gates considered. NAND operation can be better understood with the help of the following equation. These equations are written in the form of NAND gate operations.

B. HALF ADDER DESIGN WITH CMOS TRANSMISSION GATES

CMOS transmission gates used to design the half adder circuit. The transmission gate is made up of both, PMOS and NMOS transistors are connected in parallel. Both transistors are connected in parallel sequence.

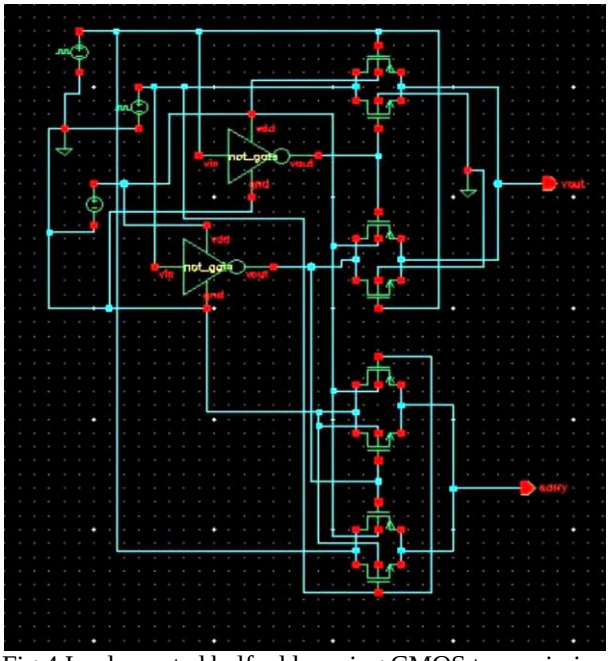

Fig.4 Implemented half adder using CMOS transmission gates [1].

Transmission gate, can conduct in both directions and control or blocked a voltage source.

A strong 0 is passed by NMOS transistors, but a weak 1 is not. A strong 1 is passed by PMOS transistors, but a weak 0 is not, and both transistors PMOS and NMOS are active on the same time. Two field-effect transistors are composed of a transmission gate, the source potential and substrate(Bulk) potential is not connected internally, due to opposition of FETs.

Two transistors, the NOT gate are connected with the MOSFET gate terminal, and the PMOS and NMOS are connected in parallel connection on transistors, only drain and source terminal. The source connection connected with the substrate terminal, resulting causing the transistor to reverse.

Substrate connection is connected with the source point, a transistor is connected in parallel, causing the transistor to reversing. The supply voltage is connected with substrate terminal, for confirmation that the substrate is always operated the reverse bias direction. The supply potential connected with n-channel MOSFET's substrate potential and the positive supply potential connected with the p-channel MOSFET's.

C. IMPLEMENTED HALF ADDER USING 2:1 MUX ON CADENCE VIRTUOSO

NMOS pass transistor logic to create the 2:1 MUX in this project. Pass transistors logic design doesn't need to connect PMOS and NMOS in parallel. As shown in Fig.5 designed a half adder in cadence virtuoso using a 2:1 MUX.

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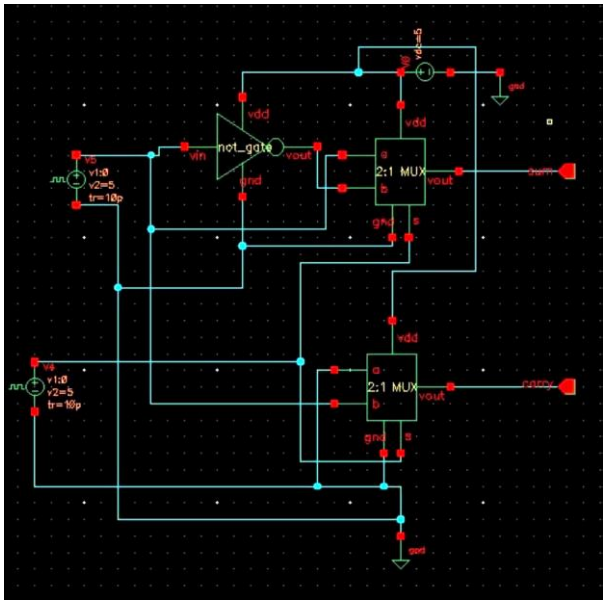

Fig.5 A half adder implemented using NMOS pass transistors logic on cadence virtuoso [1].

Pass transistors are single field-effect transistors (FETs) that pass a signal between the drain and source terminals. Pass transistors required less area and fewer routing resources. For this application, NMOS is preferred over the other two polarities. The reason for this is that electron mobility is nearly twice that of holes. As a result, NMOS switches faster than PMOS of the same size.

A strong 0 is passed by NMOS transistors, but a weak 1 is not.

A strong 1 is passed by PMOS transistors, but a weak 0 is not.

Parameter	CMOS NAND LOGIC	CMOS TRANSMISSION GATE LOGIC	NMOS PASS TRANSISTOR LOGIC
Technology	180nm	180nm	180nm
Supply voltage	5v	5v	5v
Propagation delay	Sum=24.8ps,Carry=34.48ps	Sum=1.71ps,Carry=8.05ps	Sum=1.27ps,Carry=7.7ps
Power consumption	290.5µW	135.4µW	114µW
No. of Transistors	20	12	10
Rise time(input 10ps)	Sum=22ps,Carry=26ps	Sum=24ps,Carry=25ps	Sum=21ps,Carry=19.6ps
Fall time (input 10ps)	Sum=24ps,Carry=18ps	Sum=19ps,Carry=16ps	Sum=24ps,Carry=22ps
Width of transistor	pmos =4µm,nmos=2µm	pmos =4µm,nmos=2µm	pmos =4µm,nmos=2µm

Table.2 Comparison of various half adder circuit parameters implemented design styles [1].

D. DESIGN OF HALF ADDER USING AVL TECHNOLOGY

Combinational circuit design half adder that performs the two binary digits at arithmetic operation. It is a required building block in the design of any VLSI system. A traditional half adder circuit design for power optimization is a technique used in low voltage applications half adder circuit design using Adaptive Voltage Level (AVL) techniques. When compared to conventional design circuits, AVL techniques consumed less power. AVL techniques, the ground potential raises with the help of adaptive voltage level at ground (AVLG) techniques, the supply potential raises with the help of adaptive voltage level at supply (AVLS) [2]. Using both techniques the half adder circuit design required 9T transistors.

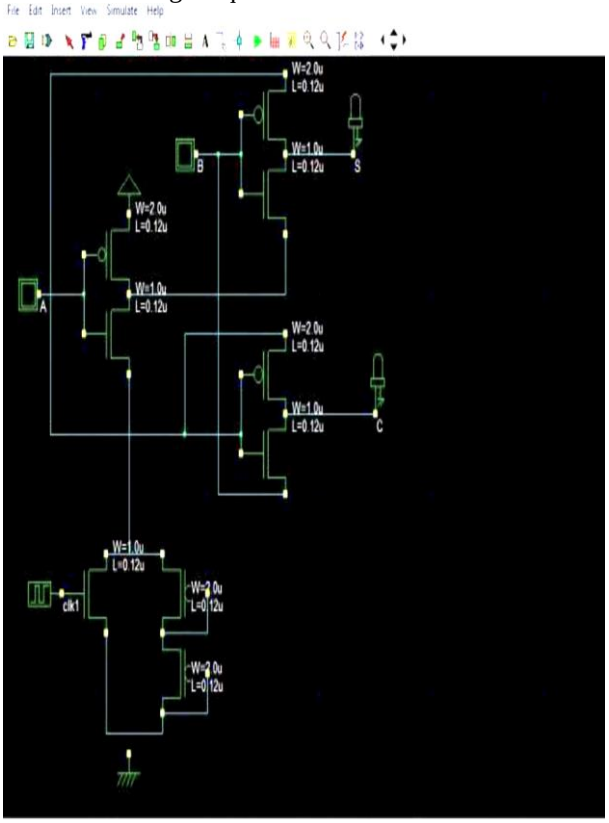

Fig.6 Half Adder Circuit diagram using the AVLG Techniques [2].

Micro wind 3.1 software simulates the cell layout design of a conventional half adder at 65nm technology using AVLG techniques and VDD=1 at 27° C. When compared to CMOS and conventional Half Adders, this design consumes less power, has a shorter propagation delay, and takes up less space on the layout. Layout cell, Simulation result, MOS characteristic, and Power vs Supply Voltage Variation [2].

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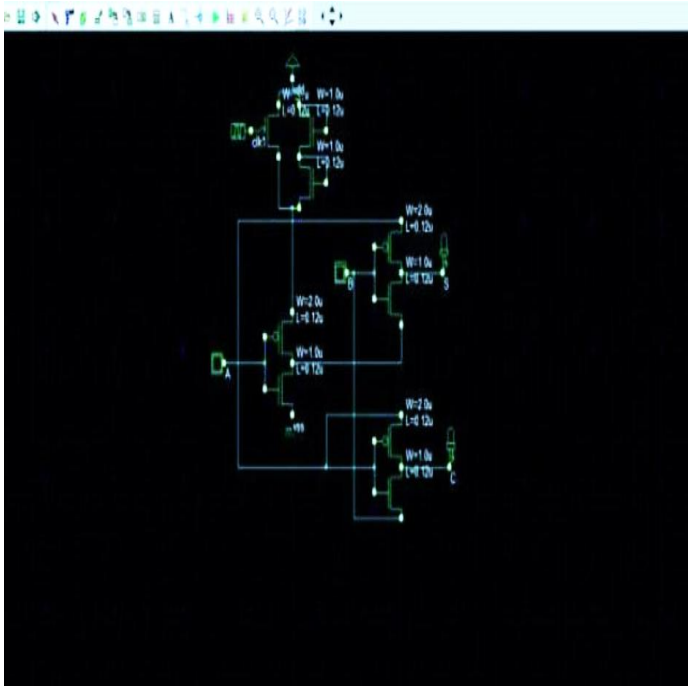

Fig.7 Half Adder Circuit Diagram Using AVLS Techniques [2].

E. HALF ADDER DESIGN USING CONVENTIONAL TECHNIQUES

The circuit is designed using a Transmission Gate and an XOR/XNOR based on the conventional design of a Half Adder. The Design style that necessitates fewer transistors. The Half Adder is implemented using only 6 transistors in this design. To implement the Half Adder, three PMOS and three NMOS transistors are required, which is significantly less than three CMOS transistors.

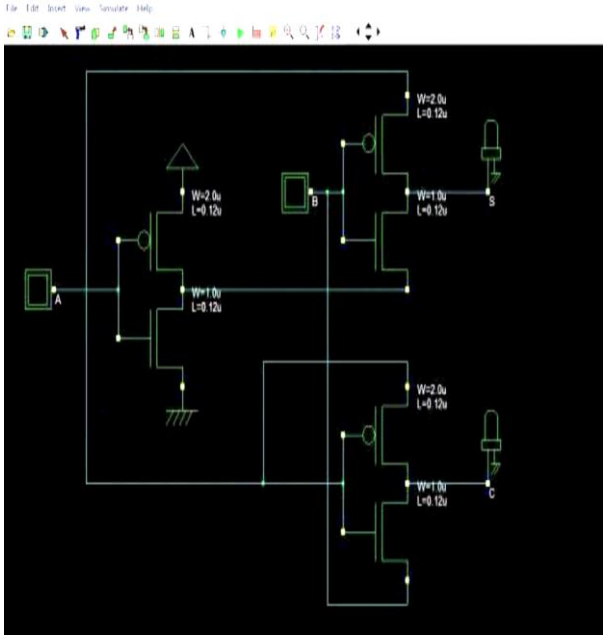

Fig.8 Half Adder Circuit Diagram Using Conventional Techniques [2]

S. No.	Parameter	Conventional	AVLG	AVLS
1.	Power consumption()	0.502	0.383	0.321
2.	Routed wires	14	35	30
3.	Compiled cell	6/6	9/9	9/9
4.	Layout area	96	136	128
5.	Propagation Delay	0.67	0.65	0.54
6.	No. of N-MOS AND P-MOS transistors	3,3	5,4	4,5

Table.3 Differences of various half-adder design parameters using conventional and AVL techniques [2].

F. HALF ADDER DESIGN USING 3-T TRANSISTORS

Using the fewest (3-T) transistors implement the half adder circuit design bases on half-adder design using 3-T transistors. To achieve the desired output, the W/L ratio is varied [3]. The combinational circuit of half adder performs the addition of two numbers. The combinational circuit half adder doesn't use the only arithmetic logic unit (ALU), processers, computers, chips but also use it in the other parts where they are used to calculate.

At the circuit, architectural, and system levels, a combinational circuit of half adder design to reducing the power dissipation. The gates count per chip area is constantly increases, the gate switching energy doesn't decreases at the same rate as gate count. In VLSI technology the power dissipation and heat removal is are difficult and more expensive. VLSI circuit that enhances the circuit operating point with the help of transistors.

The W/L ratio increase as the drain-to-source current increase. As W/L ratio rises, so does the response time. The W/L ratio is roughly proportional to the resistance. The PMOS should have a higher W/L ratio than NMOS. Increase the size of the MOSFET on the output side.

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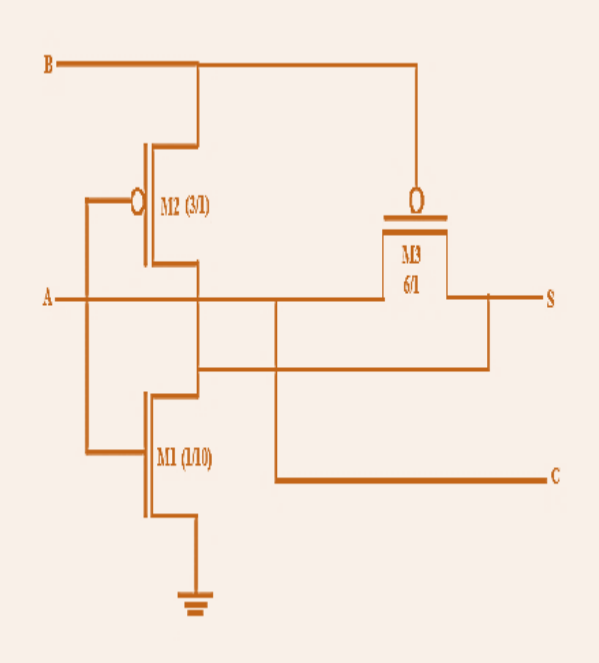

Fig.8 Half adder design using 3-T transistors [3].

Half adder circuit design using 3-T transistors with the fewest transistors possible. The speed of the circuit is increased by using a 3-T half adder. We reduce propagation delay, power, efficiency, accuracy, and power consumption by using this circuit.

A	B	S	C
0	0	0V	0V
0	1	4.49V	504.73mV
1	0	4.37V	-155.41mV
1	1	1.0V	4.96V

Table.4 Output of 3-T transistors half adder circuit [3].

III. CONCLUSION

The above study and analysis various techniques that the power consumption is reduced. Using various techniques optimized the speed of the circuit. Design of half adder using AVL technology, Design of a 3-T Half Adder, NMOS pass transistors circuit design of half adder using 2:1 MUX techniques batter than conventional techniques, the reason behind it these techniques provide high circuit speed, less propagation delay, less power consumption, batter power efficiency and accuracy. Using conventional design techniques the circuit needs fewer number the routing resource. Using a 3-T transistor circuit reduce the circuit layout area. If you optimize the circuit we have more circuit complexity, but it's a faster operating circuit and operating on low voltage.

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